Improvement in SNR with SFDR of Sigma Delta ADC for SDR Mobile Receiver

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Abstract— To increase the productivity in various sectors, foundation can be made based on mobile communication solutions to different problems. SDR is the preferred technology to stitch together advanced services for ubiquitous global mobile connectivity. We have investigated in the present study the Sigma Delta ADC, one important component of SDR. Improvement in Dynamic Range including the SFDR with a oversampling process have been shown in the presence of real life imperfection. It also gives better SNR for SDR mobile receiver. Various features of a wide band high linearity Sigma Delta ADC have also been described.

Keywords- Sigma Delta ADC, Software defined radio (SDR), Spurious free dynamic range (SFDR), Oversampling process, Signal to noise and distortion ratio (SNDR)

I. INTRODUCTION

In the last few years SDR has entered into the commercial market place. ADC is the main building block in SDR architecture. For all types of ADC, there are three universal performance parameters, sampling rate, resolution and power dissipation. ADCs usually consist of a sampler before the quantizer.

The demand for new telecommunication services requiring higher capacities, data rates and different operating modes have motivated the development of new generation multi-standard wireless transceivers. In multi-standard design, sigma-delta based ADC is one of the popular choices. In an ideal quantizer represented by staircase function, involved error is expressed as sawtooth function. This is obtained in terms of LSB = Fs/N as integral non-linearity.

Some of the asymptotic properties of quantization error are signal to noise and distortion ratio (SNDR), Error Waveform and spectrum, spurious free dynamic range and Energy conversion spectrum aliasing etc. There is a demand of ADCs with bandwidths in the MHz range and dynamic ranges over 70 dB. Also, this performance should be achieved with low power dissipation, in order to allow long battery life in portable devices. Sigma-Delta ADCs can deliver high performance with low power consumption over signal bandwidths in the MHz range, and hence it is the ADC architecture of choice in many wired and wireless receivers [4]. There are two possible realizations of a Sigma-Delta modulators, first the traditional one is Discrete-time (DT) realization, based on switched capacitor (SC) circuitry. And the second one is continuous-time (CT) realization getting popularity for wideband modulators. The power dissipation of ADC provides high resolution and linearity while using only a low-resolution quantizer by taking advantage of oversampling and noise shaping. There are three key design parameters: (1) quantizer resolution; (2) order of loop filter; (3) oversampling ratio (OSR). Increasing any of these improves the resolution under ideal conditions. However, there are limitations associated with each design parameter. In a wideband modulator, the OSR cannot be too high, as the amplifier in that case will dissipate too much. To meet demanding design targets with low OSR, high quantizer resolution and loop filter order are required.

In addition, the quantization noise spurs may affect the performance. The effects of quantization noise is to be minimized. For a specific environment, the required dynamic range is a function of the received signal power, interference power and input noise. It can be expressed as

\[ \text{Dynamic Range}_{\text{required}} = [-10 \log_{10}(\frac{C}{N_{T,C} + \sum_{k=1}^{K} I_k})] + \text{SNR}_{\text{min}} \text{dB} \]

\[ C = \text{Received signal power} \]

\[ N_{T,C} = \text{total input noise power from thermal noise sources and channel noise} \]

\[ I_k = \text{power of a particular interference} \]

\[ \text{SNR}_{\text{min}} = \text{minimum SNR required to ensure proper waveform performance} \]

Some practical effects such as aperture noise and harmonics limit a data converter’s ability to achieve ideal performance. Now, its our fortunate techniques to mitigate these effects developed. They help to reduce harmonics and AGC to ensure better Full Scale Range utilization. Samples of input signal are random, zero-mean, and uniformly distributed across quantization levels over the full scale range (FSR) of the ADC. The features of Sigma delta ADC are discussed in section II. SFDR is discussed in section III. Results are in section IV and at last conclusion of the work is in section V.

II. SIGMA DELTA ADC

Sigma Delta modulation methods have evolved through a number of generations to become one of the most attractive and popular technique for realizing high resolution, high
performance analog-to-digital (ADC) and digital-to-analog (DAC) converters. Sigma Delta modulation exploits oversampling and digital signal filtering to produce a high resolution digitized output.

Although GSM requires over 100dB of dynamic range, WCDMA requires less than 80dB, and 802.11 a similar amount. This means that it is possible to exploit the noise shaping inherent in the modulator to get the required dynamic range. We illustrate this with a second order modulator. The dynamic range can be approximated by knowing the order of the modulator, the oversampling ratio (OSR), and the number of bits of quantization (N):

\[ DR = 6.02N + 1.76 - \log(\text{OSR}) \]

For a clock rate of 200MHz and a bandwidth of 200kHz for GSM, the calculated dynamic range is over 140dB. For WCDMA at the same clock rate and with a 4MHz channel, the calculated dynamic range is 80dB which will meet the requirements. For a single bit quantizer and a 20MHz channel for WLAN, the calculated dynamic range is 45dB. This is not enough, so the solution is to raise the clocking rate or increase the number of bits or both.

In combination with the principle of oversampling, a sigma delta converter applies noise shaping in the modulator to further reduce the quantization noise within the band of interest. Some of the ADC parameters are Timing jitters, SFDR, SINAD, Effective number of bits etc., which effects the performance of ADC. We will discuss here the Spurious Free Dynamic Range (SFDR) in detail in section III. Results are in section IV and conclusion of the work in section V.

III. Spurious Free Dynamic Range

For a sine wave input without noise, uniform quantization results in pure harmonic distortion. The difference in power between the desired signal and the most powerful distortion component is termed as the spurious-free dynamic range (SFDR).

The SFDR is an important specification for spectrum analyzers, because a user cannot distinguish between distortion components and true input signals. It is also relevant for receivers, because the SFDR may limit receiver sensitivity [5]. This parameter is very important for Sigma delta ADC.

Increasing the resolution of the quantizer increases the SFDR. But the resolution of analog-to-digital converters (ADCs) is limited by the required sampling rate and the maximum allowable power consumption [6]. Analytical formulas for distortion components are available, but they are difficult to evaluate and do not easily translate to the SFDR. Therefore, system designers would benefit from simple design equations for the SFDR to allow for the exploration of the design space and optimization between resolution, SNR, and SFDR. The SFDR of a uniform quantizer, when quantizing a sinusoid without noise, increases by roughly 8 dB/bit, which was found by numerical evaluation of exact formulas and verified by simulations. This trend and the seemingly random deviations around it were mathematically explained. Adding noise decorrelates the quantization error from the input signal and, therefore, increases the SFDR. For Gaussian noise, the SFDR quadratically increases with the standard deviation of the noise in LSB. A numerical comparison between a simple approximation formula that has been introduced in this brief, and the exact value obtained from existing but complicated analytical formulas, shows an error of less than a few decibels, which is often acceptable for practical purposes. In the case of \( N \) tones, the SFDR is expected to increase by \((6 + 2N)\) dB/bit, which was derived in the same way as for the single-tone situation. These results can be applied to the design of systems without having to use the exact formulas. This can save a lot of time and effort. The results relate the SNR, the SFDR, and the number of quantization levels, and knowing two of them allows easy calculation of the third [7].

We determined the SFDR through numerical evaluation and verified by simulation for a full-scale sinusoid with \( \hat{A} = 0 \) for all even values of \( n \) (to keep symmetry around zero) up to 13 bits. For all bits, the solution is to raise the clocking rate or increase the number of bits or both.

In this section, we are going to explore the possibility of using the SFDR to provide a direct measure of the quality of the ADC. The SFDR of a perfect ADC of this (ENOB) number of bits.

\[ \text{SFDR} = 8.07b + 3.29 \text{ [dB]} \quad (2) \]

where \( b = \log_2 n \). Because \( n \) is not necessarily an power of 2, \( b \) is not necessarily an integer. Equations. Spurious Free Dynamic Range can also be given as

\[ \text{SFDR} = (8.03)^b + 3.29 \text{ [dB]} \quad (3) \]

where \( B \) is quantization bit.

**SNR:** Signal to Noise Ratio is the ratio, expressed in dB, is the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or dc.

\[ \text{SNR} = 10 \log(\sigma_x^2) - 10 \log(\sigma_y^2) - 10 \log\left(\frac{\sigma_x^2}{2L+1}\right) + (20L+10) \log\left(\frac{F}{F_{\max}}\right) \quad (4) \]

Where \( F_s \) is the sampling rate, \( F_{\max} \) is the highest frequency component of the input signal, \( \sigma_x^2 \) is the input signal power, and \( \sigma_y^2 \) is the quantization noise power.

**ENOB:** Effective Number of Bits is another method of specifying Signal-to-Noise and Distortion ratio or SINAD. ENOB is defined as \((\text{SNR} - 1.76)/6.02\) and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

IV. Results

Fig. 1 plots the numerically simulate SFDR for sigma delta ADC of ideal quantizer digitizing an FS sinusoid with No. of resolution bits upto 16 bits. The SFDR vary linearly with no. of resolution bits. We can also say that SNR will also \( Y \) vary 6 dB/bits. I have used here MATLAB Communication tool box for Equation no.(2). Fig 2 shows the effect of SNR with no. of bits at different values of SFDR. It shows that if we increase the no. of bits, the SNR will also increase and also the SNR increases with increased value of SFDR. So we can say that SFDR is directly proportional to SNR. Table I
gives the comparison between Actual and linear SFDR as a function of no.of bits. As we increase the No. of bits SFDR also increases. Table 2 shows that as we increase the order of Sigma Delta ADC, the SNR also increases with no. of bits.

### Table I. Comparison between Actual and Linear SFDR as a Function of No. of Bit

<table>
<thead>
<tr>
<th>Number of Bits</th>
<th>Actual SFDR (dB) (as shown in graph)</th>
<th>Linear SFDR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>19.55</td>
<td>21.29</td>
</tr>
<tr>
<td>4</td>
<td>35.41</td>
<td>39.29</td>
</tr>
<tr>
<td>6</td>
<td>51.57</td>
<td>57.29</td>
</tr>
<tr>
<td>8</td>
<td>67.53</td>
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<td>10</td>
<td>83.59</td>
<td>93.29</td>
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<tr>
<td>12</td>
<td>99.65</td>
<td>111.29</td>
</tr>
<tr>
<td>14</td>
<td>115.71</td>
<td>129.29</td>
</tr>
</tbody>
</table>

### V. Conclusion

In this paper we are evaluating the performance of sigma delta ADC with spurious free dynamic range in terms of signal-to-noise ratio, for this we are taking no. of bits in consideration. Here number of bits are considered. Special signal processing techniques can be used to improve the resolution of the measurement, by using a method called “Oversampling and noise shaping”. High resolution might be achieved without using an external ADC. By using the Oversampling process, the performance of Sigma Delta ADC is improving by a large amount. But there is a limitation that we cannot increase the number of bits more than 14.

With the innovation of advanced communication techniques like multi-input/multi-output and multi standard, multifunctioning, multiband radios, the demand is growing to provide multichannel programmable data conversion, which are pushing the performance of ADCs further in the coming years.

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### References


