Low Power Design Techniques for CMOS Circuits & Systems

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Abstract- Power consumption is a primary concern of designing integrated circuits in deeply scaled CMOS technologies. Present-day technologies possess computing capabilities that make things possible, such as real-time operations. High-speed computation has thus become the expected norm from the average user, instead of being the province of the few with access to a powerful mainframe. Power must be added to the portable unit, even when power is available in non-portable applications, the issue of low-power design is becoming critical. Thus, it is evident that methodologies for the design of high-throughput, low-power digital systems are needed. Techniques for low-power operation are shown in this paper, which use the lowest possible supply voltage coupled with architectural, logic style, circuit, and technology optimizations.

Index terms – low power design, dynamic power, static power, switching activities, Leakage power, power optimization.

I. INTRODUCTION

Power and energy consumption of digital systems may increase significantly during testing. This extra power consumption due to test application may give rise to severe hazards to the circuit reliability. Power consumption is the bottleneck of system performance. Low power design can be exploited at various levels, e.g., system level, architecture level, circuit level, and device level. This paper first gives a brief overview for low power optimization techniques at system and architecture level, then focus discussion on circuit level methods specifically state-of-the-art low power design techniques of clocking systems. Reducing power consumption has become an important issue in digital circuit design, especially for high performance portable devices. Many power reduction techniques have also been proposed from the system level down to the circuit level. In this section, some of these techniques, which are related to the design for parallel multiplier, will be presented.

II. SOURCES OF POWER DISSIPATION

The sources of power dissipation in digital CMOS circuits are composed of the following parts: switching power, short-circuit power, and leakage power, which is given in the below equation (1).

\[ P_{\text{total}} = \alpha_{\text{s1}} C_{\text{L}} V_{\text{dd}}^2 f_{\text{clk}} + \frac{I_{\text{cc}}}{f_{\text{clk}}} V_{\text{dd}} + I_{\text{leak}} V_{\text{dd}} \]  

(1)

The first term stands for the switching power, which is the power required to charge/discharge the circuit nodes. \( \alpha_{\text{s1}} \) is the node switching activity factor of the circuit, which is the average number of the node making a power consuming transition per clock cycle. \( C_{\text{L}} \) is the load capacitance, \( V_{\text{dd}} \) is the supply voltage, and \( f_{\text{clk}} \) is the clock frequency. The switching power consumption is the dominating component in digital circuits, and it can be reduced by minimizing any one or several of \( \alpha_{\text{s1}}, C_{\text{L}}, V_{\text{dd}}, \) and \( f_{\text{clk}} \) under the required performance. The second term in equation (1) represents the short-circuit power consumption due to short-circuit current. The short-circuit current in complementary CMOS circuit arises when both the pull-up network and the pull-down network are turned on at the same time during the transitions. The amount of \( I_{\text{cc}} \) is proportional to the rising and falling time of the input signals, transistor sizes and the output load capacitance. Hence, the longer the transition time for the input signals, the larger the short circuit current which results in more power consumed. The short-circuit power consumption can be lowered by optimal transistor sizing and input reordering transistors. The total average short-circuit current can be minimized by designing with equal input and output edge times. In this way, the power consumed by the short-circuit currents is less than 10% of the total dynamic power. In particular, when the supply voltage is lowered to be below the sum of the thresholds of the transistors, the short-circuit currents can be eliminated. The third term in equation (1) refers to the leakage power dissipation due to the leakage current. Though one and only one of the pull-up and pull-down networks in a static CMOS circuit is conducting in steady state, there still is a small leakage current which flows through the reverse-biased diode junctions of the transistors between the diffusion regions and the substrate. Another source of the leakage current is potentially the sub-threshold current of the transistors. Both sources of leakage caused the static power dissipation which constitutes a small fraction of the overall power dissipation in current technologies. However, with the progress of the technology scaling, the sub-threshold leakage currents will become a larger component in total power dissipation. The leakage current depends strongly on the technology, and it can be reduced by applying some techniques such as multi-threshold voltage CMOS technology etc.
III. LOW POWER TECHNIQUES

A. Supply Voltage Scaling

The most effective method to reduce the power consumption is scaling the supply voltage, as indicated by equation (1). Reducing the supply voltage can significantly reduce the power dissipation that is a quadratic function of the operating voltage. This is illustrated in figure 1, which shows the power consumption as a function of $V_{dd}$ for a 4-bit carry look-ahead adder in 0.18 μm process technology. The power consumption dependence on supply voltage for various logic functions and logic styles

![Figure 1. Power consumption for a 4-bit CLA as a function of $V_{dd}$](image)

However, reducing the supply voltage also increases the delay. The relationship between $V_{dd}$ and the delay, $T_d$, can be expressed as

$$T_d = \frac{C_{eff}}{f_{clk}} = \frac{C_{eff} \cdot V_{dd}}{f_{clk}}$$

(2)

From the equation (2), when $V_{dd}$ approaches the threshold voltage, $V_t$, the delay increases drastically, as shown in fig 2. Obviously, using this method causes the performance loss on the speed. In order to compensate for the loss in throughput at low supply voltages, several techniques can be applied such as parallel and pipelined architectures as well as modifying the threshold voltage of the devices.

![Figure 2. Propagation delay versus $V_{dd}$ for a 4-bit CLA adder](image)

B. Reducing Effective Capacitance

When the performance loss in throughput due to lowering the supply voltage is not acceptable, reducing the effective capacitance can also obtain low power consumption in CMOS circuits. The effective capacitance is defined by the product of the physical capacitance and the switching activity, which is shown as

$$C_{eff} = \alpha_{0-1} \cdot C_L$$

Where $\alpha_{0-1}$ is the node transition activity factor and $C_L$ is the load capacitance which refers to physical capacitance. The switching power consumption can be rewritten as

$$P_{Switching} = C_{eff} \cdot V_{dd}^2 \cdot f_{clk}$$

From the above equation, reducing the switching power consumption can be achieved by minimizing both of the physical capacitance and the switching activity.

Physical Capacitance Reduction:

The physical capacitance can be reduced through selecting the appropriate circuit style and optimizing the transistor sizes.

Effects of Circuit Styles:

The different circuit and logic styles result in different gate and diffusion capacitance of the transistors in a combinational logic circuit. Some of the circuit styles can substantially reduced the physical capacitance and is good for low-power operation. Figure 3 shows the relationship between the power-delay products of an 8-bit adder that was implemented in 2 μm CMOS technology with different circuit styles and the corresponding propagation delays.

![Figure 3. Power-delay products versus delay for an 8-bit adder](image)

As shown in Figure 3, the adder that was implemented by using complementary pass transistor logic (CPL) is about twice as fast as the conventional static CMOS. This is due to that CPL improves the performance of the circuit with a lower input capacitance and reduced voltage swing. Moreover, a CPL logic circuit consumes less power than a static CMOS one, for instance, the power saving for a CPL adder is about 30% compared to a conventional static CMOS adder. This improvement is mainly due to the reduction in capacitance. The performance of a full adder implemented with different circuit styles, such as conventional CMOS, transmission gate CMOS, CPL, without output swing restoration, CPL with minimum size PMOS restoration transistors (LCPL2), CPL and TG combination (CPL-TG), has been compared. This comparison reveals that the circuit styles impact dramatically on the delay and power dissipation of the circuit. The compared results indicate that the CPL-TG provides the lowest power delay product, and the LCPL2 has the second lowest power delay product. Both of them are the best suited for low-power high-performance applications such as adders and multipliers.
Transistor Sizing:

The capacitive load that originates from transistor capacitance and interconnect wiring can be reduced by optimizing transistor sizes whenever possible and reasonable. In general, increasing the transistor sizes results in a large (dis)charging current and simultaneously increases the parasitic capacitance. On the other hand, reducing the transistor sizes will result in decreasing input capacitance that may be the load capacitance for other gates and lowering the speed of the circuit. Thus, the objective of transistor sizing is to obtain the minimum power dissipation under given performance requirements. In order to explain how to make transistor sizing, let us consider a static inverter driving a load capacitance being composed of an intrinsic (diffusion) and an extrinsic (wiring and fan out) capacitances. When the total load capacitance to the gate output is dominated by the diffusion capacitance, the smallest possible sizes of the transistors should be used for obtaining the lowest power consumption. Otherwise, if the load capacitance is dominated by the extrinsic component, the power consumption first begins to decrease with increasing transistor sizes and then starts to increase.

C. Switching Activity Reduction

The dynamic power consumption of a circuit is strongly related to the switching activity of the circuit. Ref.[5]. The node switching activity in the circuit is predominantly determined by the architectural and registers transfer level. At the circuit level, one main consideration for low-power designs is the choice of the static or dynamic logic styles. The dynamic logic gates are clocked, and undergo the pre-charge and evaluation phases, which are suitable for high-speed applications at the expense of high power dissipation. Whereas the static CMOS is the best choice for low-power high-speed implementation of dedicated circuit applications like multipliers. The switching activity can be reduced by many means such as reordering input signals, no bus-sharing technique, and minimizing the glitching activity of the static circuits etc.

Minimizing Glitching Activity:

Glitches, or dynamic hazards, are unwanted signal transitions which occur before the signal settles to its intended value. Glitches can be generated and propagated in both data path and control parts of the circuits. The simulation result from the circuit simulator (Specter) was obtained under the different conditions. All input bits of Ai and Cin go up from zero to one, and all the input bits of Bi are set to zero. The spurious transitions consume extra power compared to the glitch-free scenarios. The number of spurious transitions in a circuit depends on the logic depth, input patterns, and intermediate carry signal states etc.

In some arithmetic circuits such as adders and multipliers, the glitches may result in a large portion of the switching power dissipation. The glitching activity in static circuit designs can be minimized by selecting structures with balanced signal paths and reduced logic depth. The tree structures can be applied to implement a circuit with both of the balanced signal paths and less logic depth, while the chain structures are quite the contrary. A good example in figure 5 illustrates the choice of the tree or chain structures. In the chained implementation shown in figure 4(a), the second adder computes twice and the third adder computes three times per cycle due to the finite propagation delay through the previous adders. By contrast, the logic depth in the tree case has been reduced from three to two and the signal paths are more balanced. Thus, the switched capacitance (effective capacitance) for the chained case is a factor of 1.5 larger than in the tree.

Another possible approach to eliminate the spurious transitions is to use dynamic logic circuits instead of static logic, since any node in dynamic logic circuits can only undergo at most one transition per clock cycle.

D. Leakage Power Reduction Technique

When the whole circuit or segments of it are not in use, they must quickly be switched into a sleep mode in which they almost consume no power. Still leakage current may cause some power consumption even in the sleep mode. If the circuit could be designed such that there is very low leakage current in this mode, then the lifetime of the portable application will increase dramatically. Active leakage control techniques are needed to manage the active power consumption.

A number of typical leakage reduction techniques fall in two categories, either leveraging the stack effect or increasing the transistor threshold voltage. Forcing transistors into stacks is not a scalable solution and its implementation becomes very complicated for large designs. And also these techniques can be grouped into two categories: (I) state-saving techniques where circuit state (present value) is retained and (II) state-destructive techniques where the current Boolean output value of the circuit might be lost. A state-saving technique has an advantage over a state-destructive technique in that with a state-saving technique the circuit can immediately resume operation at a point much later in time without having to somehow regenerate state. There are three main reasons for minimizing leakage current. They are (i) source/drain junction leakage current which is due the junction acts as an diode in reverse bias when the transistor is in sleep mode. I.e. in OFF. (ii) Is gate tunneling leakage current which flows through the oxide to substrate? If the gate oxide is thin, then the current increases exponentially. And the third one is (iii) sub threshold leakage current, which is a current from source to drain. It is diffusion current built by minority carriers in the channel in the MOS devices.
One of the main contributors to static power consumption in CMOS is sub threshold leakage current shown in Figure 5, i.e., the drain to source current when the gate voltage is smaller than the transistor threshold voltage. Since sub threshold current increases exponentially as the threshold voltage decreases, nano scale technologies with scaled down threshold voltages will severely suffer from sub threshold leakage power consumption.

The most well-known traditional approach is the sleep approach “Ref. [6], [7].” In the sleep approach, both (i) an additional "sleep" PMOS transistor is placed between VDD and the pull-up network of a circuit and (ii) an additional "sleep" NMOS transistor is placed between the pull-down network and GND. These sleep transistors turn off the circuit by cutting off the power rails. Figure 6 shows its structure. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively. The sleepy stack has a novel structure that combines the advantages of two major prior approaches, the sleep transistor technique and the forced stack technique. However, unlike the sleep transistor technique, the sleepy stack technique retains the original state; furthermore, unlike the forced stack technique, the sleepy stack technique can utilize high-Vth (high threshold voltage) to achieve more than two orders of magnitude leakage power reduction compared to the forced stack.

CONCLUSION

In this paper, several existing power reduction techniques are discussed and a novel circuit design technique to minimize sleep mode power consumption due to leakage power in CMOS technology is discussed. This circuit technique provides significant energy savings in sleep mode without any speed degradation or die area overhead. Moreover, it is almost independent of technology scaling and has no circuit design complexity.

REFERENCE