Encoding Schemes for Reduction of Power Dissipation, Crosstalk and Delay in VLSI Interconnects: A Review

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Abstract—This paper reviews different encoding schemes for reduction of power dissipation, crosstalk noise and delay. Crosstalk is aggravated by enhanced switching activity which is often main cause for the malfunctioning of any VLSI chip. Consequently, delay and power dissipation also increases due to enhanced crosstalk. Reduction in switching activities through coupled transmission line results in enormous reduction of power dissipation, crosstalk and delay. The researchers therefore often concentrate on encoding schemes that reduces the transitions of the signals. This paper reviews all such encoding schemes.

Index Terms—VLSI, CMOS, Interconnects, Encoding, SoC.

I. INTRODUCTION

The factors which affect the performance of the VLSI chips are Power dissipation, Crosstalk, Delay and Noise. Dynamic power is mainly due to the charging and discharging of the capacitive load. The dynamic power dissipation is due to switching activity in a CMOS circuit. Power can be reduced by intercommunication and interconnect optimization by data encoding technique. Crosstalk effect has two categories, Crosstalk glitches and Crosstalk delays. The magnitude of glitches depends on the ratio of coupling capacitance to the line to ground capacitance. Although crosstalk delay is also created by the same coupling effect among interconnect lines but it can be produced even if line drivers are balanced. A interconnect can be modeled in two ways, RC and RLC model. There are various encoding techniques to reduce the power dissipation, crosstalk, delay and noise in interconnect. The main sources of noise are: interconnect cross capacitance noise, charge sharing noise, charge leakage noise, power supply noise, and mutual inductance noise. These noises create unwanted deviation in currents and voltages at various nodes in the VLSI circuits (Bayoumi et al. 2005) [1].

II. ENCODING TECHNIQUES FOR REDUCTION OF POWER DISSIPATION

Low Power Coding (LPC) is used for reduction of self-switching or coupling power in address bus and data bus. Encoding schemes in address bus utilize the behavior of regularity and sequentiality property.

Burleson et al. [2] proposed an encoding scheme known as Bus Invert (BI) coding. In this scheme, entire buses are used for encoding purpose and include a redundant bit along with bit line. This encoding scheme is simple and effectively minimizes the switching activities. Similar to this encoding scheme, Partial Bus Invert (PBI) is proposed by Shin et al. [3]. In this scheme, a partial bus data are encoded in place of entire bus. Yoo and Choi [4] advanced PBI by proposing Interleaving PBI code. In this scheme the bit width and group of lines are dynamically changed. Further, PBI is again extended with Decomposed Bus Invert coding (DBI) proposed by Hong et al. [5]. In this encoding the bus lines are grouped into any arbitrary number of groups and each group is considered separately for BI coding. The SILENT technique is proposed by Lee et al. [6] to reduce power dissipation in the serial line. In this technique, data is encoded as XOR between the continuous data words. In the receiver side, original transmitted data word can be recovered by XOR of encoded word and previously decoded words. Transition skewing coding scheme proposed by Akil et al. [7] reduces power dissipation and area. This scheme deals with crosstalk, peak energy and current, switching and leakage power, repeaters area, signal integrity and noise. The authors used 90nm technology to simulate. This method of coding is efficient for the energy and area with low encoding and decoding latency overhead. The work has been further extended in 90-nm encoding scheme [8] considering 2-GHz global clock frequency. Kalyan et al. [9] proposed an encoding scheme to minimize on-chip interconnect energy consumption. The authors transmit the data using variable cycle transmission method based on the delay savings achieved through variable cycle transmission methods at regular intervals. Duvall, Chen and Nooshabadi [10] proposed a memory-less encoding scheme. They implemented this scheme for 8-bit bus in 65nm CMOS technology. They also present the 11-wire solution. The same circuitry of encoder and decoder has been used for the buses of 16, 32 and 64 bits and produced the same result.

III. ENCODING TECHNIQUES FOR REDUCTION OF COUPLING POWER

In the deep submicron technology (DSM), inter-wire capacitance and crosstalk are the major problems which cause power dissipation. The coupling capacitance not only depends on the structural and other characteristics...
like wire length, wire spacing, wire width etc but also on the data transitions \((0 \rightarrow 1, 1 \rightarrow 0)\) for below 0.25μm technology. The crosstalk effect on the line depends upon the transition of its neighboring wires. Depending upon the transitions crosstalk type can be defined. Let \(L_{i-1}, L_i, L_{i+1}\) be the three lines. There are four types of crosstalk (Type-1, Type-2, Type-3 and Type-4). Type-1 crosstalk happens if either \(L_{i-1}\) or \(L_{i+1}\) changes state. Let the coupling capacitance for this type of crosstalk is \(C\). A Type-2 crosstalk happens if \(L_i\) is in opposite state transition with one of its neighbor wires. The coupling capacitance for type-2 will be \(2C\). A type-3 crosstalk happens if \(L_i\) goes to opposite state transition with one of its neighbors and there is no change in the other. The coupling capacitance for the Type-3 will be \(3C\). A Type-4 crosstalk will happen if all three wires move to opposite state with respect to each other and with the previous state. It has maximum coupling capacitance i.e. \(4C\). Type-2, Type-3 and Type-4 are worst case crosstalk. The technique of transition pattern coding scheme (TPC) for reduction of coupling power in the data bus with encoding was proposed by Sotiriadis and Chandrakasan [11]. In this scheme, an additional bus line is added. It creates transition matrix for selecting codeword patterns such that neighboring bus line changes values in the same direction. Thus coupling capacitance and inter-wire energy is reduced. This scheme is suitable for smaller buses. The author also proposed to split the entire bus line into smaller groups and, apply TPC on these smaller groups. Xie et al. [12] studied the bus grouping method in TPC and applied genetic algorithm for grouping and found more energy saving. Zang et al. [13] proposed an encoding scheme odd/even bus-invert code. In this scheme, the authors considered the numbered bus line and also the coupling capacitances will charge and discharge by the activity of the neighbors, one line will be odd and other neighbor line will be even. The coupling activity can be minimized by controlling the odd and even line transitions separately. There are four possible conditions (i) no bus lines are inverted (0 0), (ii) only odd lines are inverted (1 0), (iii) only even lines are inverted (0 1) or (iv) all lines are inverted (1 1). In the encoding scheme the toggling sequences \(01 \rightarrow 10\) and \(10 \rightarrow 01\) are not considered, dissipating four times more energy as compared to any other transition. Muroyama et al. [14] proposed variable length coding compression scheme. In this scheme, variable length coding was extended to reduce the self capacitance switching power. Probabilistic information is used for assigning the code. The smaller length code is assigned for more frequent data. The variable length encoding scheme increases the bit width which is not very practical. Brahmbhatt et. al. [15, 16] proposed adaptive low power encoding scheme based on weighted code mapping (WCM). Mapping is based on probabilistic distribution of the source data. A window based adaptive encoding algorithm is proposed. Another encoding scheme is proposed in which WCM algorithm is combined with delayed bus algorithm [17]. The hybrid WCM and adaptive hybrid schemes show improvement upon BI, OE-BI and delayed bus algorithm. Jayaprakash et al. [18] proposed partitioned hybrid encoding (PHE). In this encoding, bus is partitioned and energy efficient encoding scheme was applied separately on each partition. Decision of application of encoding scheme is based on dynamic programming. PHE scheme provided 4 to 13 times more power saving than BI and OE-BI. An algorithm proposed by PadmaPriya et al. [19] reduces the transitions due to capacitive crosstalk. In this algorithm the author uses two extra bits for the coding of data of any bit width. Pandey et al. [20] proposed an encoding scheme to reduce the power dissipation in the NoC. The communication requirement is not fulfilled by bus architecture. The authors proposed the crosstalk avoidance code for reduction of crosstalk in NoC, so that the energy dissipation can be minimized.

### IV. Encoding Techniques for Reduction of Capacitive Crosstalk Delay

The delay in the long buses highly depends upon the coupling capacitance between the lines. Crosstalk effect takes place when the neighbor lines signal transit in opposite directions simultaneously. Capacitive crosstalk occurs when the cross coupling capacitance is comparable to or higher than the loading capacitance. For such a transition, delay may be twice or more than that of wire transition. Type-4 and Type-3 have worst delay characteristics as compared to Type-2 and Type-1. Selective skewing of bus data signal [21], transistor sizing [22], and repeater sizing is used by few authors to reduce the capacitive crosstalk. Earlier works [22-25] proposed the model, based on delay on bus. In these models, delay is introduced. This kind of model is applicable on single or pair of bus line. Sotiriadis et al. [26] proposed a delay on bus model. In this model an intentional delay is introduced in the bus according to the individual line signal. This encoding scheme eliminates the type-3 and type-4 transitions. Self-shielding code (SSC) was proposed by Victor and Keutzer [27]. This scheme eliminates type-3, type-4 and some part of type-2. The original data width ’n’ is taken and data is encoded into the bit width of ‘m’ where \(m<2n\). This approach will be extended by introducing shield wires [28-29]. The purpose of this encoding scheme is to avoid transition in opposite direction in the adjacent lines. Crosstalk aware interconnect (DYN) is proposed by Li et al. [30]. It uses the faster clock and dynamically controls the number of cycles required for transmission. The controlling of number of cycles is based on delay required for the transmission. This is done by the crosstalk analyzer. It compares the previous data sent with the current data to be sent with the help of pattern recognition to find out the crosstalk types. It uses the multiple short clock cycle in place of long clock cycle without using any encoding schemes. The DYN has less complexity and overhead as compared to SSC [28], a double spacing scheme and shielding method [31]. DYN provides better result as
compared to SSC, DBS and SHD schemes. It has less area overhead as compared to SSC, DBS and SHD. Further, the performance of DYN can be increased by using BI coding. Sainarayanan et al. [32] proposed a scheme to minimize the delay and energy consumed in interconnects. In this encoding technique, authors used 8-bit data and encode it into 9-bit data. It is stored in 9-bit register and XOR’d with forthcoming data bits for the reduction of worst crosstalk. For delay minimization the authors used wire tapering with encoding. The results shows that encoding scheme reduce delay and the encoding with wire shaping, delay reduces further for different interconnect dimensions. A high data rate asynchronous bit-serial link for long-range on-chip communication is presented by Dobkin et al. [33]. In this paper, they have shown that data bit cycle time is equal to a single gate delay, enabling 67Gbps throughput in 65-nm technology. The authors’ present links using differential dual-rail level encoding (LEDR), and current mode signaling over low-crosstalk interconnect layout. Mc Laughlin et al. [34] proposed a new architecture for the family of Asynchronous protocol converters that translate between two and four-phase protocols. It facilitates robust system design using efficient global two-phase communication and local four-phase computation. This converter circuit is implemented and evaluated on 0.18 micron TSMC process. The authors have estimated that the latency and stabilization time of original FIFO converter system will be reduced to 1.8ns (former 2.9ns) and 5.6ns (former 6.7ns), respectively. It is beneficial in comparison to the LEDR proposed earlier.

V. ENCODING TECHNIQUES FOR REDUCTION OF POWER AND CAPACITIVE Crosstalk EFFECT

Low energy set scheme (LESS) proposed by Baek et al. [35] uses XOR-XNOR (XON type) or XNOR-XOR (XNO type) operation to transmit data. In XON technique, the bus is divided into the group of 4 bits and performs the XOR operation on most significant 2 bits of current data with the previous data. The XNOR operation is performed on least significant 2 bits with the previous data. The use of XON and XNO depends on the encoding rule defined by the behavior of bit sequence to minimize the energy-delay and self-switching on the bus. The LESS technique provides better result in power, energy and delay as compared to BI encoding scheme. The encoding scheme EN_shield-Ip proposed by Lyuh and Kim [36] takes the probability graph (shows probability of transition between all possible n-bit source words) as an input. Assuming a code length of m-bit (m > n), it creates a codeword graph ensuring that there is no type-4 crosstalk. For each input data the suitable code is found out, which is an NP-complete problem. This scheme consumes less power than original data or any other schemes like BI and shielding scheme while eliminating worst case crosstalk delay. Sridhar et al. [37] proposed an overlapping coding which is a type of partial coding technique that divides the bus into sub-channels. The two adjacent sub-channels overlap at their boundary. If ‘m’ and ‘n’ are the number of code bits and data bits respectively in the sub-channel, then n data bits are mapped to the central m-2 bits of the code-words, and the boundary bits of data-words form the boundary bits of code-words. This technique eliminates crosstalk delay by using forbidden pattern overlapping codes [38] to avoid overlapping from causing crosstalk delay in the boundary bits. This scheme does not use any shielding wires. An encoding scheme is proposed by Khan et al. [39]. In this scheme, the incoming data is encoded such that the type-3 and type-4 crosstalk can be eliminated. The encoding scheme is based on the intrinsic property of 4-bit sequence. A 4-bit bus can have sixteen 4-bit sequences (4-tuples). If any one 4-tuple is modulo-2 summed with the functions Z1 (0101) and Z2 (1010) and compared with remaining 4-tuples, it will be observed that one of the two XOR’d data will have no type-4 switching with respect to the remaining fifteen 4-tuples. This encoding scheme is implemented for 0.18-μm CMOS technology. The variable cycle transmission technique is improved by Mutyam et al. [40]. The author’s aim is to minimize crosstalk delay by applying temporal redundancy (VCTR). This scheme reduces the cost of crosstalk analyzer hardware. When the crosstalk is detected, the data is encoded in two words; each word is transmitted with smaller delay, instead of delaying the transmission as in [30]. The overall delay produced by this scheme is less than delay produced in [30]. VCTR also achieves lower delay and energy consumption as compared to original variable cycle transmission technique as in [30]. Wang et al. [41] proposed a 6b9b encoding scheme to reduce the crosstalk and reduction of active power consumption single ended interconnect. This encoding scheme reduces the power consumption and was developed to avoid toggling of neighbor signals at same time. Another method which include deassembler/sembler at the sending and receiving end is proposed by Hsieh et al. [42] for designing of high performance processor. Only seven extra bits are required for 128-bit line while 85 extra bits are required for the same data line in the work of Victor and Keutzer[27]. Multi-bit Quaternary Current-Mode Signaling (MQCMS) system is proposed by Venkatraman et al. [43]. In this system, two digital signals transfer over one interconnect using current levels on 130nm IBM CMOS process. The results show data rates of 2.3Gb/s/ch to 1.15Gb/s/ch and energy of 0.19pJ/b to 0.57pJ/b for wires of 1mm to 5mm and also, two times reduction of energy per bit as compared to insertion of repeaters for 5mm wires. Srinivas et al. [44] proposed encoding scheme using memory-less code to avoid crosstalk, error correction and energy saving. The number of wires being 35% of fundamental bound. It uses low swing signaling, 10mm 32-bit bus in 0.13-μm CMOS technology. The hamming error control code is examined by Rossi et al. [45] and found that no power saving is possible by among different hamming codes.
Then a novel technique, Dual Rail, is proposed. This technique provides the energy reduction with proper bus layout. Nigussie et al. [46] proposed Level Encoded two-phase Dual Rail (LEDR) encoding. It provides delay insensitive high performance long on-chip communication using LEDR encoding. Throughput of 1-Gbps is achieved per one pair of dual rail wire at 5mm length. Less power is consumed less then 800µW at 11mm length of wire. The delay due to worst case switching crosstalk is reduced 3 fold as compared to bundled-data encoded mode. This encoding scheme is simulated in 130 nm CMOS technology. A spatio-temporal bus encoding scheme is proposed by Avinash et al. [47] to minimize the crosstalk effect. The proposed scheme eliminates the worst case crosstalk among the interconnect wires thereby reducing delay and energy consumption. This scheme has a built-in error detection capability without any performance overhead. The authors have focused on L1 cache address/data bus of microprocessor in 90-nm and 65-nm. This paper also compared the proposed encoding scheme with other various encoding schemes. A new encoding scheme i.e. Phase-encoding was proposed by D’Alessandro et al. [48]. Self timed communication is based on phase modulation of a reference signal. A reference signal can be sent on the number of transmission line and the data can be recovered by observing the sequence of events on the lines. The number of lines will increase. To reduce this problem the authors have proposed the new encoding algorithms which generates symbol dependent matrices. These matrices are used to control the phase of transmission line. Type-2 and Type-3 cross coupling are eliminated in this scheme. Courtey et al. [49] proposed a convolutional encoder for crosstalk reduction (CECR). It is useful for reduction of delay, power and noise for on-chip buses. Results shows that power consumption reduction reach up to 12% for 10mm bus in 65 nm technology and more if buses are longer. It also allow to increase the data propagation of 20% and the reduction of overall worst noise case transitions of 51%.

VI. ENCODING TECHNIQUES FOR REDUCTION OF INDUCTIVE AND CAPACITIVE CROSSTALK EFFECT

Inductive coupling becomes more effective on the busses operating at high frequencies in DSM. It increases wire delay [50-51] similar to capacitive crosstalk. Signal overshoot and undershoot may damage the devices. The inductance in the power and ground can increase the noise in the supply and ground voltage when large current flows. This problem is known as ground-bounce problem. Inductance effect cannot be neglected in high performance circuits especially in global interconnect. Kaushik et al. [52] discussed about voltage scaling for crosstalk reduction in CMOS driven interconnects. In this paper, effect of crosstalk in voltage scaled interconnects is discussed. Authors considered two adjacent bus wires, flowing current in the aggressor line. It creates two different noise signals in the victim line. One signal will flow in the same direction is known as forward crosstalk and other will flow in the opposite direction is known as backward crosstalk. Backward crosstalk is created due to inductive while forward crosstalk is created due to capacitive crosstalk. In the high frequency circuit inductive coupling dominates the capacitive coupling. The worst case coupling occurs when the adjacent wire signal transit in opposite state in the RC circuit model while, in the RLC circuit model worst case coupling occurs when all wire transition in the same direction. To reduce inductive crosstalk an encoding scheme modified bus invert (MBI) scheme is proposed by Lampropoulos et al. [53]. This scheme inverts the data pattern to minimize transition in the same direction. The bus lines are grouped into pairs and each pair of adjacent line as well as their previous values are the inputs of the logic cell (L-cell). It encodes the values occurring in the pair of the bus line to reduce the inductive coupling. The MBI scheme reduced more crosstalk as compared to BI and CBI for the 8-bit bus. A similar encoding technique is proposed by Tu et al. [54] utilizing the BI to remove the inductive effects. In this proposed technique the input data is inverted when the number of transitions in the same direction is more than half of the number of bus line. The encoding scheme provides good results to reduce the worst coupling effect when the buses are about micrometer long and work above GHz frequency. Another encoding scheme proposed by Raghundan et al. [55] uses selective bit inversion and shield bit insertion to reduce inductive crosstalk delay and simultaneous switching noise (SSN). In this scheme, input data is broken into chunks of 4-bits and this chunk is coded as two 3-bit data tuples. Two tuples are sent in two successive cycles. SSN check is used to determine if two or more simultaneous transitions are occurring for a set of 3-bit with previous data. If SSN checker does not detect two or more simultaneous transitions then first 3-bits of 4-bit chunk are sent in the first cycle. Fourth bit, shield and coding bits are sent in the next cycle. If SSN checker detects two or more simultaneous transitions then the invert of the 3-bit of a 4-bit chunk is sent in first cycle and a high impedance state as a coding bit value. Using high impedance state in place of ‘1’ for coding bit will not allow any current flow. It will reduce both power and inductive coupling effects. Lin et al. [56] proposed the encoding scheme for nanometer technology to reduce the LC crosstalk coupling. The authors assumed that in coplanar bus structure, each driver has uniform size and symmetry such that the effective output resistance is same for both rising and falling signal transitions. A valid code set is generated with the help of parameters of wires and data bit. The valid code set has minimal total transition power to map the data patterns. Raun and Tsai [57] proposed a low power dynamic bus encoding scheme known as Dictionary-based segmented inversion (DSI®) scheme. This encoding scheme reduces capacitive and inductive effects by the measurement of real RLC model.
CONCLUSION

In this review paper, various encoding schemes have been reviewed. It is observed that with the rise in VLSI technology, complexity of encoding schemes have increased. The main emphasis of different researchers is to reduce the signal transitions in the bus. The different types of crosstalk are generated due to the transitions in the signals and this crosstalk is the main cause of the power dissipation, delay and noise. Researchers have suggested various schemes to curb down the effects of crosstalk from micrometer to nanometer technology.

REFERENCES


