A Novel FPGA Based Incremental Encoder Interface Circuit

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Abstract — Design of incremental encoder interface involves designing a circuit to decode the positional and directional data embedded in the output signal of the encoder, as well as designing a counter circuit to count the number of pulses. This can be done either by using a custom IC or 5-10 discrete ICs. Four monostable circuits would be needed to implement the direction sensing unit. However, with the increase in number of components, system reliability is reduced. Also, system is easily susceptible for interference by noise. This paper presents a way of implementing the above functions both in hardware and software. In addition, the paper provides a mechanism for efficient error correction, thus making it suitable for servomotor control design, even under noisy condition. As FPGA based design offers better performance over cost ratio while microcontroller based design offers better price with acceptable performance, the paper explains the design using FPGA prototype.

Index terms — Biphase, Control system, Encoder reader circuit, Error correction, Forward pulse train, FPGA.

I. INTRODUCTION

Whenever mechanical rotary motions have to be monitored an encoder is the most important interface between the mechanical and the control unit. Encoders transform rotary movement into a rotation are detected by a single channel, a second signal, phase shifted by 90 degrees is also generated. This second signal, along with the first signal, enables the direction of rotation to be determined.

Fig. 1 Typical Encoder waveform showing Channel B being 90° offset from Channel A.

II. PROPOSED SCHEME

The change of states of signal A and B of Fig. 1 can be represented in the form of the following state diagram:

An incremental biphase encoder is the most commonly used device in computer – controlled feedback system. The microcomputer actuates several final control elements based on the information obtained from the encoder. In addition to providing positional and directional information, the encoder interface circuit must also perform some special function to maintain proper operations, such as missing pulse correction, error correction, resetting the position counter based on control signal from the microcomputer etc. It requires 5-10 discrete ICs to implement all the above functions[1]. Also certain types of combinational logic are error prone due to gate delay or threshold offsets and multivibrator imprecision. This paper tries to reduce drastically the amount of hardware needed by using the FPGA based design. The Proposed Scheme is explained in Section II, Design details are given in Section III and Section IV explains the Simulation results.
The above state diagram has been formed taking the value of channel A as the msb (most significant bit) and the value of the channel B as the lsb (least significant bit). The state transition from 00 → 01 → 11 → 10 is denoted by FPT (forward pulse train) and state transition from 00 → 10 → 11 → 01 is denoted by RPT (reverse pulse train)[2,3]. The above state diagram has been used to obtain the following state model: A counter is incremented at every forward transition and decremented at every reverse transition of the signal A and B. Thus the value of the counter at any instant gives the total number of edges detected.

### III. Implementation Of Algorithm

The design of the above algorithm is shown in Fig. 3. Here the whole operation is divided into two parts:

1) Controller Part
2) Data Part

The controller part takes care of the state transition. This state transition depends on the value of the channels A and B, as given in the edge detection algorithm.

The Data part is nothing but a counter. This counter increment with forward transition and decrement with reverse transition of signal A and B. Here a three bit up – down counter is shown.

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**Fig. 3**: Design of Incremental Encoder Circuit

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* All the 'x' terminal are connected to the Up counter and 'y' terminal to the Down counter.

* Assume all the flip flop are connected to the master clock

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The Program was stimulated using Modelsim XE III 6.1.[4,5] The snapshot of the simulation is shown in the Fig.4. The channel A and B are the input of the encoder reader circuit. With the positive edge transition of the clock pulse, the state of the encoder changes. At first, for a full clockwise rotation, the counter indicate the value four in the state S1. In the similar way, the value of the counter decrement due to anticlockwise rotation.

Fig.4: Snapshot of the Simulated waveform in the absence of noise
V. CONCLUSION

The Design, Implementation and Simulation results of Incremental Encoder Interface using FPGA have been presented here. Here we find the design of the controller requires 7- discrete ICs only as compared to 10 ICs using conventional design, and the data path depend on the designer. Using this implementation, the system reliability can be increased thus making it a favorable tool for automatic control system.

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