Analysis of Timing Jitters on the Performance of Bandpass DT-Sigma Delta ADC for Software Defined Radio Receivers

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Abstract: In the present scenario, wireless technologies require an advanced receiver which supports multi-standard and multi-mode transmission. In an ideal software radio, the data conversion process occurs immediately after the antenna in the receiver chain. A/D conversion at an early stage plays an important role for achieving such flexibility at the receiver. Bandpass sampling allows for the digitisation of bandpass signals at RF or intermediate frequencies. The sampling process is never ideal, and many factors limit performance. One factor is Timing Jitters (aperture jitter and clock jitter) of the sample-and-hold function of the ADC. This results in a variation of the sampling period from one sample to another, degrading performance. This effect becomes more serious as sampling occurs at higher carrier frequencies. This paper investigates the effects of timing jitter in bandpass sigma delta ADC sampling systems, and describes how oversampling the information signal has an impact on the effects of jitters and also gives evaluation of the performance in terms of SNR and draw mean error power spectrum due to aperture jitter as well as clock jitter.

Keywords: Band pass Sigma Delta ADC (ΣΔ) Modulators, Clock jitter, Aperture Jitter, Software defined radio (SDR), Signal to Noise Ratio.

I. INTRODUCTION

Wireless communications receivers have generally adopted a super heterodyne architecture for its superior performance. However, the number of components required can be considerable, and with the concept of reconfigurable radio currently being developed, the need for more flexible transceiver architectures is necessary. A software radio (also called a “flexible architecture radio”) is one of the most important emerging technologies for the future of wireless communication services because of traditionally analog functions of a radio receiver will be replaced with software or digital hardware [1]. This is desirable for reconfigurable radio systems, where, as many radio functions as possible should be defined in software to create a flexible transceiver. Sigma Delta techniques are also applicable to the high resolution A/D conversion of band pass signals using band pass sigma delta modulators. Sigma delta ADCs have been integrated with digital signal processor(DSPs) and some extra digital hardware dedicated to performing a portion of the decimation. However, the effects of timing jitters limit the sampling at high carrier frequencies.

In the past years, the demand for high speed and low power wire-line and wireless an application has favored the use of oversampling Delta-Sigma ADC (Analog-to-Digital Converters) due to their better speed-accuracy tradeoff. ΣΔ ADCs is perceived as the promising candidate for implementing digital bandpass conversion. Unfortunately, since the sampling process now occurs at higher frequency, the probability of the clock jitter and aperture jitter are arise and introduce the significant timing error.

II. TIMING JITTER IN BANDPASS SIGMA DELTA ADC

Sampling at higher frequencies using conventional Nyquist sampling would require rates of over twice the carrier frequency, which would result in a very large number of samples, and hence require a lot of computational power for further processing. The alternative is to intentionally alias the signal by sampling at rates which are significantly less than the carrier frequency. The original signal can be recovered if the band pass signal is sampled at greater than twice its information bandwidth[4]. Bandpass sampling has the advantage of down conversion without the use of mixers. The basic transfer function for the sigma-delta modulator can be easily developed using the linear model in Figure 5 where the quantizer error is modeled as an additive noise source and $H(z)$ is the transfer function of the integrator.

![Figure 5. Signal Flow of the Sigma-Delta Modulator](image-url)
Assuming that the quantization noise is zero, the output signal, the signal transfer function that is

\[ STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} \quad \ldots (1) \]

By assuming that the input signal is zero, the noise transfer function that is

\[ NTF(z) = \frac{Y(z)}{E_{q}(z)} = \frac{E_{q}(z)}{1 + H(z)} \quad \ldots (2) \]

We can see that the signal transfer function is simply a delay, while the noise transfer function is a discrete-time differentiator. Clock jitter mainly caused by the instability of the oscillator resulting in sampling time errors in the ADC, therefore degrading the converter’s achievable SNR and resolution[3]. Aperture jitter stands for the random sampling time variations in ADCs which are caused by broadband noise in the sample-&-hold circuit

\[ SNR \text{ in case of jitter} \]

\[ SNR = 10 \log \left[ \frac{P_{\text{signal}}}{P_{\text{jitter}} + P_{\text{quant}}} \right] \text{ dB} \]

Where Psignal represent the power of input signal, Pjitter and Pquant indicate the jitter- triggered error and quantization noise, respectively

\[ SNR_{\text{vco}} = 20 \log \left[ \frac{1}{N} \sum_{n=0}^{N-1} S_{ss}(f)(1 - e^{-2\pi f^2/\text{vcoT}}) \right] \quad \ldots \ldots (3) \]

where Sss(f) represent the PSD of input signal, vco represent oscillator instability.

The effects of aperture on \( \Sigma \Delta \) ADC can be predicted by the following simple analysis.

\[ SNR_{\text{aj}} = 10 \log \left[ \frac{1}{2} \int_{-\infty}^{\infty} S_{ss}(f) df \right] \]

\[ \left( \frac{1}{2} \right) \sum_{n=0}^{N-1} S_{ss}(f)(1 - e^{-2\pi f^2/\sigma_{aj}^2}) df \]

\[ \ldots \ldots (4) \]

III. SIMULATION RESULTS

In order to confirm the above analysis, some simulation result is presented. In Figure (1), over sampling is expected to improve the system performance by spreading out the quantization noise to a much larger bandwidth. However, this improvement can only be perceived for the low value of OSR. In Fig (2) as we increase input frequency, SNRaj is increasing but due to presence of jitter, SNR is decreasing and we get SNR in between 50 to 55dB. Fig.(3) Shows that aperture jitter power spectrum. Which are uniformly distributed over the whole digitized band. The signal was sampled with a sampling frequency of 400 MHz and white Gaussian aperture jitter with a Standard deviation (rms aperture jitter) \( taj = 0.25 \text{ ps for } fi << taj^{-1}. \) The error power spectrum is white. Fig(4) shows that clock jitter’s power spectrum which has narrow peaks at \( \pm 20\text{MHz} \) and \( \pm 90\text{MHz} \) surrounded by Lorentzian shaped spectra which are spread across the spectrum of input signal. The chosen phase noise constant \( fi << (\text{vcoT})^{0.5} \)
IV. CONCLUSION

This paper presents how degradation in the system performance due to Timing jitter (clock jitter and aperture jitter) by showing simulation graphs ant. In the case of clock jitter the characteristic functions strongly depend on the absolute sampling time. This time-varying behavior is caused by the non-stationary of the clock jitter process. Error power spectra of clock jitter and aperture jitter are significantly different. In the case of aperture jitter the mean error power is uniformly distributed over the whole digitization band, so that the jitter dependent SNR in a given frequency band can be increased by oversampling techniques. In the case of clock jitter the error power is concentrated around the frequencies of the input signal components. Thus, oversampling does not help to increase the SNR. Analysis shows that Clock jitter are dominating error, severely degrades the system performance in terms of achievable SNR.

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<th>JITTER TOLERANCE</th>
<th>WLAN=wireless local area network</th>
<th>DVB-H=Digital Video Broadcasting – Handheld</th>
<th>UMTS=Universal Mobile telecommunication Services</th>
<th>GSM=Global System for Mobile</th>
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V. REFERENCES