An Efficient Adiabatic Circuit Design Approach for Low Power Applications

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Abstract— An alternative and efficient design for static adiabatic logic gates based on the GFCAL adiabatic family is proposed. The GFCAL circuit proposed earlier had made use of diodes for controlling the charging or discharging of the output node. A method is proposed to replace the diodes and thus make the circuit more energy efficient by avoiding the break-in voltage drop across the charging and discharging paths. Simulations of the circuit on HSPICE have been carried out and it has been observed that the replacement of diodes indeed lowers the power consumption of the circuit. Other gates have also been studied and efficiency of these compared to conventional CMOS gates is found to be to the tune of 60%.

Index Terms— Low Power Design, Adiabatic Design, Arithmetic circuits

I. INTRODUCTION

Adiabatic circuits are those circuits which work on the principle of adiabatic charging and discharging and which recycle the energy from output nodes instead of discharging it to ground. Conventional CMOS circuits achieve a logic ‘1’ or logic ‘0’ by charging the load capacitor to supply voltage $V_{dd}$ and discharging it to ground respectively. As such every time a charge-discharge cycle occurs, an amount of energy equal to $CV_{dd}^2$ is dissipated. Unlike the conventional CMOS circuits, in adiabatic circuits energy is recycled. Instead of discharging the load capacitor to ground, the charge is discharged to the power supply. Since the charge has to be discharged to supply, the supply in adiabatic circuits is a time varying one called the power clock. It has been observed that among the different waveforms for charging or discharging the load capacitor, a ramp is more efficient and as such trapezoidal power clocks have been used in many adiabatic circuit styles. Many adiabatic logic circuits which dissipate less power than static CMOS logic circuits have been introduced as a promising approach in low power circuit design. Drawbacks of many of the proposed techniques include need for multi-phase power clock supplies, differential inputs and corresponding high complexity of the logic blocks. In this paper adiabatic gates with non-differential inputs and a single power clock have been proposed. The idea behind the circuit is built upon the basic diode based circuit proposed in [1] and [2].

II. DIODE BASED ADIABATIC LOGIC

Figure-1 shows the circuit for diode based static adiabatic inverter as given in [1] & [2]. The working of this inverter is simple and straight forward. When the input is logic ‘0’ the PMOS turns ON, NMOS turns OFF and the branch consisting of M1 and D1 allows the charging of the load capacitor when the clock is going from 0 to $V_{dd}$.

![Figure-1 Diode based adiabatic (GFCAL) circuit](image)

When the input is logic ‘1’, the NMOS turns ON and allows discharge of the load capacitor to the supply when power clock goes from $V_{dd}$ to 0. The main drawback of this design is the use of diodes in charging or discharging paths. Since a diode has a voltage drop of $\gamma V$, the break-in voltage of the diode across it, if a charge of magnitude q is passed through it then energy equal to $\gamma qV$ is expended in the process. Our method of design reduces the power dissipation by replacing the diodes with MOS transistors. The difference here is that the transistors are not diode connected and their turning ON or OFF is controlled by the power clock.

III. PROPOSED ADIABATIC LOGIC

Figure 2 shows a schematic of the proposed new logic style. Unlike the working of diode based circuit, here four cases have to be considered as explained here. First let’s consider that the load capacitor is in uncharged state and input is logic ‘0’. In this case, the transistor M1 turns ON and when the clock goes from 0 to $V_{dd}$, M3 turns ON starts charging the capacitor. When the clock goes from $V_{dd}$ to 0, M3 turns OFF at some point and thus prevents discharging.
In another case when the output is ‘1’ and input is ‘0’, the circuit remains in the same state as before. So a ‘0’ at the input gives a ‘1’ at the output. Consider the situation when input is ‘1’ and the load capacitor is already charged to ‘1’. In this case, M2 turns ON and when the clock waveform changes from $V_{dd}$ to 0, the transistor M4 also turns ON and allows the discharge of the charge stored in the capacitor to the supply. In the case when the capacitor is not initially charged, an input of logic ‘1’ does not affect the output conditions. This design is made on the assumption that the transistors turn ON and OFF satisfactorily giving the required waveforms. For this to happen, the substrates of the transistor should be biased appropriately. The biasing part of the circuit is discussed in the next section.

A. Biasing the circuit for proper operation

Figure 3 shows the biasing scheme used to make the circuit operate satisfactorily. Since the substrates of transistors are to be connected to most positive or negative voltage (depending on whether its PMOS or NMOS), and here the supply is a varying one, we have connected the substrates of the PMOS transistors to capacitors which are charged to and remain at $V_{dd}$. This part of charging the biasing capacitors happens only once when the circuit is turned on and thus will not be responsible for any power dissipation. The substrates of NMOS transistors are grounded.

The inverter circuit was simulated using HSPICE with device libraries of 180nm technology. The circuit has been found to work satisfactorily up to input frequency of 100MHz. The speed of the circuit can be improved by taking a smaller load capacitor. But it comes at the expense of higher ripple in the output waveform. So a trade-off has to be made between ripple of the waveform and speed. The output levels of ‘0’ and ‘1’ also deteriorate as the speed of the circuit is increased. For 50MHz, the observed output logic levels were 0.5V for ‘0’ and 3.0V for ‘1’ (figure 4). These values are acceptable and it has been verified that cascading of multiple stages is possible.

The transmission delay when gates were cascaded was observed to be directly related to the time period of the power clock. Faster power clock gave lesser transmission delays. The minimum delay between two stages was found to be equal to one cycle of the power clock. The power clock should be comparatively faster than the input signal. But increasing the frequency of the clock has a drawback viz. The power consumption increases due to faster switching of the transistors. A clock frequency of about 5 or 6 times that of input frequency has been found to be satisfactory. The energy dissipation has been found to be 2.64pJ/cycle. The diode based circuit shown in figure 1 is simulated to compare the performance of the proposed circuit. The energy dissipation in this case is found to be 3.22pJ/cycle which is almost 13.5% higher than that of the proposed circuit. The observed waveforms shown in figure 4 are explained by deriving approximate mathematical expressions. This is discussed in the next section.

A. Approximate Expressions for Output

The output waveforms observed are explained based on approximate expressions derived by treating the transistors as ideal switches with finite resistance $R$ when ON and open circuited when OFF. A load capacitance of value 200 femto-Farad was taken. The trapezoidal clock waveform varies in between 0 and $V_{dd}$ has equal rise-time and fall-times of $T$.

With these assumptions, the voltage equation when the output node is charging is given by

$$V_c(t) = \frac{V_{dd}}{T}(t - RC) + V_0 e^{-\frac{t}{RC}}$$  \hspace{1cm} (1)

The equation when the output node is discharging is given by

$$V_c(t) = V_{dd} - \frac{V_{dd}}{T}(t - RC) + V_0 e^{-\frac{t}{RC}}$$  \hspace{1cm} (2)

The energy given by the power supply while charging the load capacitor is

$$E_{charging} = \frac{1}{2} \frac{(V_{dd})^2}{R} \frac{2t^3}{3} - C \left( \frac{V_{dd}}{T} \right)^2 \frac{t^2}{2} - \frac{V_{dd}V_0}{T} C e^{-\frac{t}{RC}} (t + RC)$$  \hspace{1cm} (3)

and the expression for energy given by power supply while the load capacitor is discharging is given by
\[
E_{\text{discharge}} = \frac{V_i^2}{R} \left( \frac{t}{2T} - \frac{t}{3} \left( 1 - \frac{t}{T} \right)^{\frac{3}{2}} \right) - \frac{V_0^2}{RT} \left( \frac{t}{3} - \frac{RCt^2}{2} \right) + \frac{V_i V_f}{T} RCE \frac{t}{\sqrt{RT}} (RC + t)
\]

and \( V_i, V_0 \) in the above equations are the constants depending on the initial conditions before the charging or discharging cycle. It can be seen that the energy consumed for charging is inversely related to the rise time and fall time \( T \) of the clock waveform. Ideally the waveform should have amplitude in the range of 0 to 3.3V but due to the threshold voltages required for turning ON of transistors, the output values are 0.5V and 2.9V. Although the output swing was less, the design was still found to be cascadable. A chain of 100 inverters were simulated and it was found that the output levels are maintained throughout the chain.

V. OTHER LOGIC GATES

An implementation of NAND and NOR gates is shown in the figure 5 (a) and (b). These gates work on the same principle as the inverter circuit. Any gate can be implemented using the pull-up and pull-down circuits of conventional CMOS structure. Average power consumed by different circuits subject to the same set of input test vectors was compared to that of CMOS. Table 1 gives a comparison of power consumed by different gates. It is seen that the efficiency of current design method is up to 60% compared to CMOS.

VI. CONCLUSION

From the results of simulation it has been observed that the replacement of diodes (or for that matter diode connected MOS devices) with switches controlled by power clock significantly reduces the power consumption of the adiabatic circuit. Other advantage is the complexity of fabricating a diode is avoided. The biasing circuit is universal and can be used for all gates on a given chip. The efficiency of previous design approach as given in [1] was 50% compared to CMOS. So this method improves the efficiency by 10%. The efficiency obtained further depends on the supply voltage used and device parameters like threshold voltage as evident from the approximate expressions derived.

REFERENCES