High Speed Parallel and Reconfigurable VLSI Implementation of 2-D DWT

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Abstract— An efficient high-speed VLSI implementation of the Discrete Wavelet Transform (DWT) based on hardware-efficient parallel FIR filters has been proposed in this paper. High speed 2-D DWT with low computational speed and high throughput with controlled increase of hardware cost is proposed. Fast algorithm based parallel FIR filter structures are designed to improve the processing speed and control the increase of the hardware cost at the same time. This paper also introduces two new FPGA based parallel implementation of DWT using convolution scheme. The first implementation uses parallel processing to increase the speed of the algorithm. The second architecture is a novel reconfigurable DWT architecture in terms of wavelet filters and wavelet decomposition structures. Our implementation support both Orthogonal and Bi-Orthogonal filters of variable length.

Keywords— DWT, Very-Large-Scale Integration, Parallel FIR structures, Fastconvolution, Reconfigurable.

I. INTRODUCTION

Discrete wavelet transform has a huge number of applications in science, engineering, mathematics multimedia and image compression[1]. The most popular schemes in discrete wavelet transform namely the filter bank scheme and the lifting scheme. Traditionally, Fourier transforms have been utilized for signal analysis and reconstruction[2]. However, Fourier representations do not include any local information about the original signals. On the basis of streaming processors such as graphics processing unit, [3,4] have arrived at a versatile conclusion that filter bank approach outstands lifting scheme in current generation graphic processing units. An efficient architecture for convolution based DWT that has several optimization techniques is presented in [5]. In [6] they have proposed an efficient architecture for 2D DWT in which resources where shared and reused. But the storage element used in them increased the memory required. A comparative study of the general modified recursive pyramid algorithm and symmetric pipeline is performed in [7]. Pipelining though increased the throughput increased the latency which proved to be inefficient in real time applications of DWT. In [8] they have proposed a parallel FIR filter implementation. Conventionally DWT are implemented by filter bank method [6]-[17]. Some recent proposals [2-7] addressed the importance of flexibility and proposed programmable or reconfigurable DWT architectures for either variable wavelet filters [2-5] or variable wavelet decomposition structures [6-8]. Reconfigurable structures are parallel systems that are designed around multiple general-purpose processors and multiple field programmable gate array (FPGA) chips. These systems can leverage the synergism between conventional processors and FPGAs to provide low-level hardware functionality at the same level of programmability as general-purpose computers. Hybrid Reconfigurable Computing Environment is one of the first general-purpose reconfigurable machines combining the flexibility of traditional microprocessors with the power of Field Programmable Gate Arrays (FPGAs. SRC-6E Reconfigurable Computer is one example of this category of hybrid computers [10].

II. PROPOSED ARCHITECTURE

For computing an NxN image the 1-D DWT of each row first is computed followed by the computation of columns [11]. To explain our proposed filter length of 4 and image size of 6x6 is assumed. The coefficients of high pass are a,b,c,d and the low pass coefficients are l,m,o,p.

\[
X = \begin{bmatrix}
x_{00} & x_{01} & x_{02} & x_{03} & x_{04} & x_{05} \\
x_{10} & x_{11} & x_{12} & x_{13} & x_{14} & x_{15} \\
x_{20} & x_{21} & x_{22} & x_{23} & x_{24} & x_{25} \\
x_{30} & x_{31} & x_{32} & x_{33} & x_{34} & x_{35} \\
x_{40} & x_{41} & x_{42} & x_{43} & x_{44} & x_{45} \\
x_{50} & x_{51} & x_{52} & x_{53} & x_{54} & x_{55} \\
x_{60} & x_{61} & x_{62} & x_{63} & x_{64} & x_{65} \\
x_{70} & x_{71} & x_{72} & x_{73} & x_{74} & x_{75}
\end{bmatrix}
\]

By applying the inputs parallel the two inputs can be fed parallel, here for eg (x_{02},x_{00}) and (x_{03},x_{01}) are fed at first clock period. Throughput is increased twice by the proposed architecture. Fig.1. represents a 2-parallel FIR filter with coefficients \{b,d\}.

The above block diagram can be represented by applying the ISC based convolution as follows:

\[
Y_2 = P_2^T \ast H_2^T \ast Q_2^T \ast X_2
\]

\[
H_2 = \text{diagonal} \ [b \ b+d \ d]
\]
This paper has introduced an idea, that if, the inputs to the subfilter are made parallel the complexity can be reduced and the speed can be increased. Parallel FIR subfilter is represented as a shared filtering core in which the subfilter are shared among the parallel FIR filters.

III. RECONFIGURABLE STRUCTURE

Variable instances of DWT kernels and various types of filters can be used in the implementation of this module. As shown in fig. 2, other requirements for multimedia processing systems include high throughputs for real-time processing and an efficient scheme to ensure high quality reconstruction of the compressed data.

Our design facilitates the implementation of a wide range of DWT filters such as: Daubechies (DAUB1, DAUB2, DAUB10), Haar, Symlets. An external memory is required to buffer the data and this external memory is connected to the reconfigurable processing element array and reconfigurable address generator. The processing element performs the filter operation, will be different and so will be the combination of them. External memory required for the reconfigurable processing element array consist of a PLA, which store the default hardware configuration and the RAM which stores the values according to the different wavelet filters used. The reconfigurable structure is shown in figure 3.

In [12] a design method is employed in which they utilized lifting scheme to perform DWT analysis. Though lifting scheme is more advantageous than convolution in terms of fewer computational resources high end parallelism cannot be achieved due to the data dependencies exhibited by lifting scheme. The long critical path also adds on to the disadvantage of lifting scheme. Any DWT filter can be chosen and after convolution and dependence graph formation the computational resources are mapped into systolic array. The folding technique will induce feedback loop from the output to input. Feedback registers buffer the feedback signals from the feedback loop.

IV. HARDWARE IMPLEMENTATION

To implement high speed vlsi architecture a fast convolution along with parallel FIR filter is proposed. The fast convolution is based architecture, which reduces the stronger operations like multiplications at the cost of weaker operations.
like delay and adders is implemented. Addition operation is implemented using carry save adders while coefficient quantization is achieved a look-ahead maximum absolute difference algorithm (MAD)[17]. Horner’s rule [18] is employed to gain accuracy during CSD multiplication. Second stage parallel FIR structure is implemented as shared processing core to reduce cost. Two reconfigurable DWT PE are adopted to form the Reconfigurable DWT PE Array, and several useful wavelet filters and wavelet decomposition structures are stored in the PLA as default configurations.

V. RESULTS AND ANALYSIS

We targeted a Xilinx XC5VLX30 FPGA for our experiments, using ModelSim 6.0c for simulation purposes and Xilinx ISE 9.1i for synthesis. It has been noticed that as the level of parallelism increases the number of delay elements, multiplication and addition elements does not drastically increase, thereby a controlled increase in the number of elements is achieved as the level of parallelism increases. The throughput and the hardware utilization have been compared with different wavelet filters, and it have been found to be efficiently utilized.

<table>
<thead>
<tr>
<th>TABLE I. PERFORMANCE ANALYSIS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wavelet Filter</td>
</tr>
<tr>
<td>(5,3)</td>
</tr>
<tr>
<td>(9,3)</td>
</tr>
<tr>
<td>(9,7)</td>
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<tr>
<td>(2,10)</td>
</tr>
<tr>
<td>(13,7)</td>
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</tbody>
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<table>
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<tr>
<th>TABLE II. COMPARISON OF THE NUMBER OF DELAY ELEMENTS, MULTIPLICATION AND ADDITION ELEMENTS USED</th>
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<tbody>
<tr>
<td>LEVEL OF PARALLELISM</td>
</tr>
<tr>
<td>---------------------</td>
</tr>
<tr>
<td>4</td>
</tr>
<tr>
<td>8</td>
</tr>
<tr>
<td>12</td>
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<tr>
<td>16</td>
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VI. CONCLUSION

The regularity and the simplicity in the control signals of the FIR structures have been exploited for an efficient VLSI implementation. Higher processing speed along with less critical path can be achieved when parallel FIR structures with higher parallelism levels are used. Less complex, more efficient, parallel FIR filter were designed using FFA, quantization process and area reduction techniques. Parallel filters required 45% less hardware compared to traditional structure. The proposed method is suitable for software and programmable DSP chips. Dynamically reconfigurable in terms of the wavelet filters and wavelet decomposition structures were implemented using convolution scheme.

REFERENCES


[12] Po-Chih Tseng, Chao-Tsung Huang, and Liang-Gee Chen,‖ Reconfigurable discrete wavelet transform architecture for advanced multimedia systems.