A CMOS Buffer without Short Circuit Power Consumption for Low Power Application

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Abstract—A new CMOS buffer without short-circuit power consumption is proposed. In this work, the gate-driving signal of the output pull-up (pull-down) transistor is fed back to the output pull-down (pull-up) transistor to get tri-state output momentarily, eliminating the short-circuit power consumption. The TSPICE simulations are used to verify the operation of the buffer. It is observed that the power-delay product of the proposed buffer is about 15% smaller than conventional tapered CMOS buffer.

Keywords—CMOS buffer, short-circuit power consumption, MOS.

I. INTRODUCTION

In CMOS integrated circuits, large capacitive loads are often encountered [1], [2], [3]. These large loads occur both on-chip, where high, localized fan-out and long global interconnect lines are common, and off chip, where highly capacitive chip-to-chip communication lines exit [4], [5], [6]. In order to drive these large capacitive loads at high speeds, buffer circuits are required which must quickly source and sink relatively large currents while not degrading the performance of previous stages [7]. With the high integration level of CMOS, the capacitive load of periodic signals such as clock has become very large. With such a large capacitive load, driving circuits consume a relatively large portion of the total power of a VLSI [8]. The power consumption of a CMOS buffer driving a capacitive load consists of dynamic switching power and short-circuits power. While the switching-power consumption is unavoidable to drive a capacitive load, short-circuit power is a waste of current and should be minimized or even eliminated for low-power operation [1].

The buffer provides a high impedance input, so as not to load down the logic/registers and high current to quickly charge (discharge) the large capacitive load. Thus, the buffer isolates the logic/registers from the load, amplifying the signal along the way [9], [10].

In past, many different approaches [4], [8], [11], [12], [13] to tapered buffer design have been described in the literature, focusing on a variety of performance aspects. The most commonly addressed criteria in tapered buffer design are propagation delay, power dissipation and physical area. Analytic expressions to determine the tapering factor and the number of stages of a tapered buffer system; these parameters are the two primary variables in the design of tapered buffers. An application-specific tapering factor and number of stages of a tapered buffer system necessary to drive a wide range of capacitive loads [14], [15], [16]. All the work focussed so far includes the short circuit power consumption. This issue is handled in our works. A conventional tapered CMOS buffer, shown in Fig.1, consumes both the dynamic switching power and short-circuits power due to simultaneous turn-on of the pull-up/pull-down transistors [17], [18], [19], [20] as illustrated in Fig.2. Short-circuit power consumption can be eliminated by tri-stating the output node momentarily before every output signal transition. In this work, we concentrated on the simulation part of the without short circuit power consumption and working on the analytical approach in our subsequent work.

Fig. 1 Design of tapered CMOS buffer

Fig. 2 Timing diagram of tapered CMOS buffer
The rest of the paper is organized as follows. In Section II, schematic and functionality of the proposed buffer is presented. The results obtained are discussed in Section III. Finally, concluding remarks are offered in Section IV.

II. SCHEMATIC AND FUNCTIONALITY OF PROPOSED BUFFER

A new CMOS buffer without short-circuit power consumption is proposed. The output pull-up and pull-down transistors are driven by separate driving signals generated so the pull-up and pull-down transistors do not turn on simultaneously. The schematic and timing diagrams of the proposed CMOS buffer are shown in Fig.3 and Fig.4 respectively.

A. Functioning of proposed buffer

The gate driving signal \( N_1 \) (\( N_2 \)) of the output pull-up (pull-down) transistor is fed back to the output pull-down (pull-up) transistor to get tri-state output momentarily, eliminating the short-circuit power consumption. The logic states of the output stage driver change only once for each output transition in the proposed buffer as opposed to twice in the FS [11] and CFS [17] buffer. Since the gate driving signals are fed back instead of the output signal itself, the feedback delay is independent of the output capacitive load, making the optimization of the circuit much easier. The pull-up and pull-down operations are explained respectively in the following.

![Fig.3 Proposed CMOS buffer without short-circuit power consumption.](image)

![Fig.4 Timing diagram of tapered CMOS buffer](image)

When the input signals IN rises from 0 to \( V_{DD} \), the internal node \( N_2 \) falls from \( V_{DD} \) to zero, turning off the output pull-down transistor \( M_2 \). Then, the node \( N_1 \) rises from zero to \( V_{DD} \) and after some delay, the node \( N_1 \) falls from \( V_{DD} \) to zero. Now, the output pull-up transistor \( M_1 \) is turned on and the output voltage begins to rise from zero to \( V_{DD} \). Since the node \( N_2 \) is driven to zero before the node \( N_1 \), the pull-down transistor \( M_2 \) is turned off before the pull-up transistor \( M_1 \) is turned on. Therefore, there is no period when both the pull-up and pull-down transistors are turned on simultaneously and thus no short-circuit power consumption. When the input signal IN falls from \( V_{DD} \) to 0, the node \( N_1 \) is driven to \( V_{DD} \), turning off the output pull-up transistor \( M_1 \). Then, the node \( N_1 \) falls from \( V_{DD} \) to zero and after some delay, the node \( N_2 \) rises from zero to \( V_{DD} \). Now, the output pull-down transistor \( M_2 \) is turned on and the output voltage begins to fall from \( V_{DD} \) to zero. Since the node \( N_1 \) is driven to \( V_{DD} \) before the node \( N_2 \), there is no period when both the pull-up and pull-down transistors are turned on simultaneously and thus no short-circuit power consumption in this case, as well.

III. RESULTS AND DISCUSSION

The proposed buffer is simulated in TSPICE simulator for two different technology nodes i.e. 180 nm and 250 nm. To see the clear cut impact of short circuit power, we have chosen 180 nm and 250 nm technology nodes. Fig. 5 and Fig. 7 plot the propagation delay vs. load capacitance at 180 nm and 250 nm technology nodes respectively. It is observed from the Fig. 5 and Fig.7 that propagation delay increases as the load capacitance increases. The propagation delay is significant in case of proposed buffer design as compared to the conventional tapered for a given load. The large no of transistors used in proposed buffer introduces large internal parasitic capacitance which require large time to charge and discharge thereby increasing the propagation delay.
Fig. 6 and Fig. 8 plot the average power vs. load capacitance at 180 nm and 250 nm technology nodes respectively. It is reported in Fig. 6 and Fig. 8 that power consumption is significantly lower in case of proposed buffer due to the absence of short circuit power consumption component. However it is shown in Fig. 9 that power delay product is improved in a proposed buffer. This means that extent of reduction in power consumption is more than the extent of delay increment in proposed buffer. Thus proposed design is suitable for the application where large capacitive load is encountered and low power consumption is required.
A new CMOS buffer has been proposed which has no short-circuit power consumption. The output pull-up and pull-down transistors are driven by separate driving stages which ensure pull-up and pull-down transistors do not turn on simultaneously. The TSPICE simulation results show about 15% improvement in the power-delay product compared to a conventional tapered CMOS buffer, and thus the proposed buffer is suitable for low-power application where large capacitive load is encountered.

IV. CONCLUSION

A new CMOS buffer has been proposed which has no short-circuit power consumption. The output pull-up and pull-down transistors are driven by separate driving stages which ensure pull-up and pull-down transistors do not turn on simultaneously. The TSPICE simulation results show about 15% improvement in the power-delay product compared to a conventional tapered CMOS buffer, and thus the proposed buffer is suitable for low-power application where large capacitive load is encountered.

REFERENCES