A New Topology for Mitigating the Common Mode Voltage in Medium Voltage Induction Motor Drives

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Abstract. In squirrel cage induction-motor (SQIM) drives, the motors are normally fed with pulse width modulated (PWM) voltages which cause spike \( (dv/dt) \) across the motor terminals. This may lead to insulation failure and damage of motor due to common mode voltage across the winding. This paper proposes a new topology for medium voltage IM drives with series connected three-level inverters to decrease \( dv/dt \) by increasing number of steps in the applied voltage. This paper also clearly explains the PWM control strategies for series connected inverters. The proposed series connected inverter topology for a squirrel cage induction motor is developed and simulated in MATLAB®/Simulink. The simulation results show the reduction in common mode voltages and validate the applicability of proposed topology for medium voltage induction motor drives.

Keywords: Common-mode Voltages, Series connected Inverters, Squirrel cage Induction motor, Pulse width modulation, Harmonic reduction.

1 Introduction

Induction motors are being used extensively in applications requiring fast and accurate control of speed and position. It is widely known that induction motors are robust, more reliable and require little maintenance. These are normally fed by the PWM converters. The PWM inverters generate common-mode voltages and can have very a high \( dv/dt \) [1]. Due to common mode voltages “motor bearing failure” and “motor winding insulation breakdown” occurs [2][3]. This problem can be eliminated by applying the multi-level voltages to the motor. A number of techniques have been suggested to reduce or eliminate the common-mode voltages, generated by the various configurations of multilevel inverters. Multilevel converters are considered today as the state-of-the-art power-conversion systems [4] for high-power and power-quality demanding applications.

Multilevel voltage profiles can also be obtained by using higher order neutral-point-clamped (NPC) multilevel inverters [10] or by cascading a number of two-level inverters [8][9]. However, these multilevel NPC inverters suffer from dc-bus imbalance [5][6][7], and unequal ratings of the clamped diodes [11] etc., which are not very serious problems for inverters with three level or lower. With the Flying capacitor
inverter it requires a huge number of capacitors. The clamping capacitor must be setup with the required voltage level. So, there is a necessity of initialization of the converter [11]. With the cascaded H-bridge it needs separate dc sources. Need to provide separate isolated dc supplies for each full-bridge converter. This paper proposes a new topology with series connected three level inverters for medium voltage induction motors which decrease $dv/dt$ by increasing number of steps in the applied voltage. In the proposed topology, the power circuit is flexible in structure, and hence, the number of modules to be connected in series depends on the power of the drive.

In this paper, the proposed topology and its sinusoidal pulse width modulation control strategies are implemented and simulated in MATLAB®/Simulink. The simulation results are presented for the series connected three level inverter topology for medium voltage squirrel cage induction motor drive applications.

2 Proposed converter topology

The proposed topology, shown in Fig.1, contains four NPC three level inverters. The output voltage of each inverter is connected to the transformers which are connected in series to produce multilevel output voltage in order to reduce the high dv/dt in output voltage. The generation of gate pulses for each of three-level inverter module is based on sinusoidal pulse width modulation (SPWM) with Phase opposition Dispassion (POD) method. The generation of modulating waves for the series connected inverters is explained in the following section.

![Block diagram for the Proposed Converter Topology](image)

If $V_{dc}$ is the dc-bus voltage of each inverter module, “$\alpha$” is the turns ratio of each transformer and “$n$” is the number of inverter modules then for sinusoidal PWM (SPWM) strategy; the motor rms phase voltage ($V_{ph}$) can be expressed as:

$$rms \ of \ V_{ph \ motor} = \sqrt{3} \times mn \frac{V_{dc}}{\sqrt{2}} \quad (1)$$

where ‘m’ is modulation index of the inverter topology (In this work, m=1).
Modulation Index (m) of the inverter is given by
\[ m = \frac{\text{Peak of Vph inverter}}{\pi \cdot \frac{V_m}{2}} \] (2)

3 Generation of modulating waves for proposed topology

The basic principle of gate pulse generation for inverters is based on the SPWM method with the reference of following equations.

\[ V_r = V_m \sin(\omega t) \] (3)

The Fig. 2 shows the modulating signals corresponding to all four inverters which are extracted from the reference modulating wave. The modulating signals corresponding to all four inverters can be expressed as given below.

The modulating signal of inverter 1,
\[ V_{r1}(wt) = V_{r1 \, pos}(wt) + V_{r1 \, neg}(wt) \] (4)

where
\[ V_{r1 \, pos}(wt) = \begin{cases} \frac{\omega t}{\sin^{-1}(\frac{1}{4})}, & 0 \leq \omega t < \sin^{-1}(\frac{1}{4}) \\ 1, & \sin^{-1}(\frac{1}{4}) \leq \omega t < \sin^{-1}(\frac{1}{2}) \\ \frac{\pi - \omega t}{\sin^{-1}(\frac{1}{2}) - \sin^{-1}(\frac{1}{4})}, & \sin^{-1}(\frac{1}{2}) \leq \omega t < \omega t < \sin^{-1}(\frac{1}{2}) \\ 0, & \pi - \sin^{-1}(\frac{1}{4}) \leq \omega t < \pi \end{cases} \]

and
\[ V_{r1 \, neg}(wt) = -V_{r1 \, pos}(wt - \pi) \]

The modulating signal of inverter 2,
\[ V_{r2}(wt) = V_{r2 \, pos}(wt) + V_{r2 \, neg}(wt) \] (5)

where
\[ V_{r2 \, pos}(wt) = \begin{cases} 0, & 0 \leq \omega t < \sin^{-1}(\frac{1}{4}) \\ \frac{\omega t - \sin^{-1}(\frac{1}{4})}{\sin^{-1}(\frac{1}{2}) - \sin^{-1}(\frac{1}{4})}, & \sin^{-1}(\frac{1}{4}) \leq \omega t < \sin^{-1}(\frac{1}{2}) \\ 1, & \sin^{-1}(\frac{1}{2}) \leq \omega t < \omega t < \sin^{-1}(\frac{1}{2}) \\ \frac{\pi - (\omega t + \sin^{-1}(\frac{1}{2}))}{\sin^{-1}(\frac{1}{2}) - \sin^{-1}(\frac{1}{4})}, & \sin^{-1}(\frac{1}{2}) \leq \omega t < \pi - \sin^{-1}(\frac{1}{2}) \\ 0, & \pi - \sin^{-1}(\frac{1}{4}) \leq \omega t < \pi \end{cases} \]

and
\[ V_{r2 \, neg}(wt) = -V_{r2 \, pos}(wt - \pi) \]

The modulating signal of inverter 3,
\[ V_{r3}(wt) = V_{r3 \, pos}(wt) + V_{r3 \, neg}(wt) \] (6)

where
\[ V_{r3 \, pos}(wt) = \begin{cases} 0, & 0 \leq \omega t < \sin^{-1}(\frac{1}{4}) \\ \frac{\omega t - \sin^{-1}(\frac{1}{4})}{\sin^{-1}(\frac{1}{2}) - \sin^{-1}(\frac{1}{4})}, & \sin^{-1}(\frac{1}{2}) \leq \omega t < \sin^{-1}(\frac{1}{4}) \\ 1, & \sin^{-1}(\frac{1}{4}) \leq \omega t < \omega t < \sin^{-1}(\frac{1}{4}) \\ \frac{\pi - (\omega t + \sin^{-1}(\frac{1}{2}))}{\sin^{-1}(\frac{1}{2}) - \sin^{-1}(\frac{1}{4})}, & \sin^{-1}(\frac{1}{2}) \leq \omega t < \pi - \sin^{-1}(\frac{1}{2}) \\ 0, & \pi - \sin^{-1}(\frac{1}{4}) \leq \omega t < \pi \end{cases} \]

and
\[ V_{r3 \, neg}(wt) = -V_{r3 \, pos}(wt - \pi) \]

The modulating signal of inverter 4,
\[ V_{r4}(wt) = V_{r4 \, pos}(wt) + V_{r4 \, neg}(wt) \] (7)
Where \( V_{r4\_pos}(wt) \) = \[
\begin{cases}
0 & 0 \leq \omega t < \sin^{-1}\left(\frac{2}{3}\right) \\
\sin(\omega t) & \sin^{-1}\left(\frac{2}{3}\right) \leq \omega t < \pi - \sin^{-1}\left(\frac{2}{3}\right) \\
0 & \pi - \sin^{-1}\left(\frac{2}{3}\right) \leq \omega t < \pi
\end{cases}
\]

and \( V_{r4\_neg}(wt) = -V_{r4\_pos}(wt - \pi) \)

From eq. (4) - (7), it can be observed that the summation of the all the modulation waves at any point of time is equals to the reference modulating wave (\( V_r \)).

\[
V_r = V_{r1} + V_{r2} + V_{r3} + V_{r4}
\] (8)

Fig. 2 Modulating waves for the four series connected inverters

4 Simulation Results

The proposed converter topology with four series connected three-level inverters for a medium voltage SQIM is developed and simulated in Matlab/Simulink. The Fig. 3 shows the line voltage and harmonic spectrum of each inverter. Fig. 4 depicts the output phase voltage of the proposed converter and the harmonic spectrum corresponding to the DC voltage of 600V for each converter. From the Fig.4, it can be observed that the proposed converter generates a better output voltage with a peak value of 2077 V and THD of only 8.66%.

The common mode voltage (CMV) can be expressed as

\[
V_{CM} = \frac{(V_{ao} + V_{bo} + V_{co})}{3}
\] (9)

Where \( V_{ao}, V_{bo}, \) and \( V_{co} \) are the phase voltages of inverters. Fig. 5 shows the common mode voltage with the proposed topology which is very small (<130V) compared to a single three level inverter (400V). The common mode voltage with different topologies of same rating is summarized in the table 1. From table 1, it can be observed that the proposed topology produces very less common mode voltage.
Fig. 3 Line voltage and harmonic spectrum of a) Inverter 1, b) Inverter 2, c) Inverter 3 and d) Inverter 4

Fig. 4 Phase voltage and harmonic spectrum of the output voltage
Table 1: Comparison of CMV with different topologies

<table>
<thead>
<tr>
<th></th>
<th>Single Three-Level Inverter</th>
<th>Series connection of three 3-Level Inverters</th>
<th>Series connection of four 3-Level Inverters</th>
<th>Single 5-Level Inverter</th>
<th>Single 9-Level Inverter</th>
</tr>
</thead>
<tbody>
<tr>
<td>% THD</td>
<td>33.62 %</td>
<td>12.22 %</td>
<td>8.66 %</td>
<td>7.89 %</td>
<td>4.71 %</td>
</tr>
<tr>
<td>Peak Voltage</td>
<td>2092 Volts</td>
<td>2073 Volts</td>
<td>2077 Volts</td>
<td>2059 V</td>
<td>2065 V</td>
</tr>
<tr>
<td>RMS Voltage</td>
<td>1479.5 Volts</td>
<td>1466 Volts</td>
<td>1468 Volts</td>
<td>1456 V</td>
<td>1460 V</td>
</tr>
<tr>
<td>CMV</td>
<td>400 Volts</td>
<td>150 Volts</td>
<td>120 Volts</td>
<td>200 Volts</td>
<td>135 Volts</td>
</tr>
</tbody>
</table>

A squirrel cage induction motor is connected to the proposed converter to validate the applicability. The Fig. 6 depicts the phase current, speed and torque developed by the proposed converter fed, medium voltage SQIM for a reference torque of 50 N-m applied at time 1 sec.
5 Conclusion

In this paper, a series connection of three-level inverters has been proposed for a medium-voltage SQIM drives with reduction of common mode voltages and decreasing the high dv/dt with increasing the number of steps in output voltage. The proposed topology has low voltage stress and low total harmonic distortion. The huge requirements of components with different ratings are eliminated and the dc bus imbalance problem will not present in this topology. The proposed inverter topology output consists of number of steps, which leads to increase the life of the motor due to decrease in dv/dt. This proposed method has an advantage even if one inverter module is failure then the topology works with reduced power level. The proposed topology for a medium voltage SQIM drive is simulated in Matlab/Simulink environment and the results validate applicability of the proposed scheme.

References