Implementation of Arctangent Computation Unit for Pedestrian Recognition System-on-Chip

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Abstract. In this paper, we implement the arctangent computation in Histograms of Oriented Gradients (HOG) descriptor extraction, targeting real-time pedestrian recognition System-on-Chip (SoC) design. Experimental results with 90nm CMOS technology shows the feasibility of the hardware architecture for SoC design.

Keywords: Histograms of Oriented Gradients (HOG), Pedestrian Recognition, Arctangent Operation, Hardware Accelerator, System-on-Chip (SoC)

1 Introduction

Pedestrian recognition has become of significant interest for the usage model such as prevention of traffic accidents by using vehicle cameras and crime deterrence by using security cameras. In order to achieve this usage model, a recognition application is required to (a) acquire the image or video stream, (b) compute descriptor vectors from the image, (c) recognize object. Among these steps (b) and (c) are the most computationally challenging tasks.

In this paper, we implement arctangent computation circuit in Histograms of Oriented Gradients (HOG) [1] descriptor extractor based on our previous research [2], targeting real-time pedestrian recognition System-on-Chip (SoC) realization with feasible hardware complexity. We first describe required computations in HOG descriptor extraction in Section 2. Section 3 proposes our hardware architecture for arctangent operation and demonstrates the implementation results using 90nm CMOS technology. We discuss the performance and hardware cost compare to other researches in Section 4 and conclude this paper in Section 5.

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2 Histograms of Oriented Gradients (HOG)

Pedestrian recognition uses feature descriptors as probability indicator of pedestrians. There are several feature descriptors that have been proposed to detect pedestrian recognition such as Harr wavelets [3], with Harr-like features [4], PCA-SHFT [5] and with Gabor filters [6]. In this paper, we chose HOG [1] descriptor for our pedestrian recognition because it is known to be an efficient features extraction scheme, is in combination with various classification algorithms, and has sufficient accuracy for our usage model of interest. HOG descriptor is a grey-level image feature formed by a set of normalized gradient histograms.

![HOG descriptor Extraction](image)

Fig. 1. Overview of HOG descriptor extraction

In the HOG pedestrian recognition scenario, we start with an input image that the recognition system takes with a camera. The intent is to extract HOG descriptors from the image. In order to do so, there are three major steps. Fig. 1 illustrates the overview of the HOG descriptor extraction, although we refer the reader to [1] for a more detailed description.

First, a 1-D spatial derivatives, \( f_x(x,y) \) and \( f_y(x,y) \), in x- and y-direction are computed by applying the gradient filters \( M_x, M_y \) to all the pixels in the image \( I(x,y) \),

\[
\begin{align*}
  f_x(x,y) &= M_x \cdot I, \\
  f_y(x,y) &= M_y \cdot I,
\end{align*}
\]

\( M_x = [-1 \quad 0 \quad 1] \quad M_y = M_x^T \) (1)

Figure 2 shows the computation of the orientation direction using the arctangent computation. The gradient magnitude and orientation direction for each pixel are computed by

\[
\begin{align*}
  M(x,y) &= \sqrt{f_x(x,y)^2 + f_y(x,y)^2} \\
  \theta(x,y) &= \tan^{-1}\left(\frac{f_y(x,y)}{f_x(x,y)}\right)
\end{align*}
\] (2)

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The next step is the histogram generation. Each pixel within the cell casts a weighted vote for an edge orientation histogram channel based on the orientation of the gradient element centered on it, and the votes are accumulated into orientation bins over local spatial regions. As a result, a histogram is generated by combining all generated histograms belonging to a block that consists of cells. Once all of the histograms within a block have been obtained, they are normalized due to the variance of gradient strengths over a wide range.

3 Implementation of Arctangent Operation

The HOG descriptor extractor operates on the grayscale images and evaluates block of 8×8 pixels, voting edge oriented gradient into 9 orientation bins in 0-180 degree. This requires the calculation of gradient magnitude and orientation direction for each pixel (See Eq. (2)). Our hardware accelerator computes the orientation direction for eight pixels in parallel.

Figure 3 illustrates the block diagram of the arctangent computation unit which consists of a LUT and eight calculation blocks. The LUT stores 90 entries, where each entry has 12bits to represent the tangent value. The arctangent block takes inputs (value and start signal), and search the corresponding degree by searching the LUT.
We adopted binary search algorithm to complete the arctangent operation in 7 cycles, which is less than the gradient magnitude calculation latency. Therefore, the multi-cycle operation of arctangent calculation unit does not slow down the overall performance of HOG descriptor extraction.

The arctangent computation unit was implemented using Verilog™ HDL and a logic description of our design has been obtained by the synthesis tool from the Synopsys™ using 90nm technology. Table 1 summarizes the physical characteristics of the arctangent calculation unit. The Synopsys™ tool chain provided critical path information for the logic up to 1.17 GHz, which is faster than system clock frequency 400MHz. And the area of circuit is approximately 0.018mm² that is feasible for on-chip integration.

| Physical Characteristics of the arctangent calculation unit |
|--------------------------|-----------------|
| Voltage                  | 1.1 V           |
| Frequency Max.           | 1.17 GHz        |
| Area                     | 0.018 mm²       |
| Dynamic Power            | 3.08 mW         |
| Leakage Power            | 0.28 mW         |

4 Discussions

Calculating the orientating direction requires calculating the arctangent function and division which is very expensive to hardware implementation as shown in Eq. (2). Hardware architectures for HOG feature extraction adopting methods to simplify the computation in order to reduce the hardware complexity, targeting FPGA implementation were proposed [7, 8]. They adopted an orientation binning scheme that determines the angular bin without computing the orientation angle explicitly. The simplified arctangent operation was implemented with comparing operations by checking the tangent values at the boundaries of bins, satisfying the following conditions.

\[ f_s(x, y) \tan \theta_i \leq f_s(x, y) \tan \theta_i < f_s(x, y) \tan \theta_{i+1} \]  

(5)

This approach reduces the hardware complexity, but it does not calculate the orientation direction exactly. In HOG descriptor extraction, votes are interpolated trilinearly among neighboring bins in both orientation direction and position to reduce the effect of aliasing as shown in Eq. (3). This requires computation of the exact orientation direction. The use of look up tables (LUTs) is a common approach but it requires large amount of memory space, eventually increasing hardware complexity. Approximation algorithms for hardware implementation usually calculate arctangent in iterative way, which increase the latency for calculation of orientation direction. Our approach uses LUT and binary search algorithm to find out the orientation direction. However, this does not slow down the performance of the overall system, by overlapping the iterative operation with the calculation of square root, which also
requires iteration. Moreover, area of our circuit is feasible for on-chip integration. In summary, our proposal enables the calculation of orientation angle to be in 1-degree precision, supporting tri-linear interpolation for superior classification performance with feasible hardware complexity.

5 Conclusions

In this paper, we implemented the arctangent computation unit, which is a sub-block of HOG descriptor extractor. Our design adopted LUT and binary search algorithm to find out the orientation direction, requiring multi-cycle operation. However, the latency for calculating arctangent is hidden by the computation time of magnitude, without slowing down the overall performance. Moreover, the proposed hardware calculates the orientation angle to be 1-degree precision, enabling the tri-linear interpolation which results superior classification performance. We plan to implement overall system for the pedestrian recognition along with RISC core.

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References