New Bridgeless DCM Sepic PFC Rectifier with Low Conduction and Switching Losses

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Abstract—New bridgeless single-phase ac–dc power factor correction (PFC) rectifier based on Sepic topology is proposed. The absence of an input diode bridge and the presence of only two semiconductor switches in the current flowing path during each switching cycle result in less conduction losses and improved thermal management compared to the conventional Sepic PFC converter. The proposed topology is designed to work in discontinuous conduction mode (DCM) to achieve almost unity power factor in a simple and effective manner. The DCM operation gives additional advantages such as zero-current turn-on in the power switches, zero-current turn-off in the output diode and reduces the complexity of the control circuitry. The proposed rectifier is theoretically investigated. Performance comparisons between the proposed and conventional Sepic PFC rectifiers are performed. Simulation and experimental results are provided for a design example of a 65-W/48-V at 100-Vrms line voltage to evaluate the performance of the proposed PFC rectifier.

Index Terms—Bridgeless rectifier, power factor correction (PFC), rectifier, Sepic converter, total harmonic distortion (THD).

I. INTRODUCTION

The Preferable type of power factor correction (PFC) circuit is the active PFC since it makes the load behave like a pure resistor, leading to near-unity load power factor and generating negligible harmonics in the input line current. Most active PFC circuits and switched-mode power supplies (SMPSs) on the market today comprise a front-end bridge rectifier followed by a high-frequency dc–dc converter. Fig. 1 shows an example of a conventional PFC Sepic and Cuk rectifiers. Referring to Fig. 1, it is clear that the current path flows through two rectifier bridge diodes and the power switch (Q) during the switch on-time, and two rectifier bridge diodes and the output diode (Do) during the switch off-state. Thus, during each switching cycle, the current flows through three power semiconductor switches. This approach is suitable for a low power range. In the low-line input and high-power applications, the high conduction loss caused by the high forward voltage drop of the bridge diode begins to degrade the overall system efficiency, and the heat generated within the bridge rectifier may destroy the individual diodes. Hence, it becomes necessary to utilize a ridge rectifier with higher current handling capability or heat dissipating characteristics. This increases the size and cost of the power supply, which is unacceptable for an efficient design. The number of component conducted at each subinterval mode is reduced in a new bridgeless power factor...
correction circuit (PFC) based on single ended primary inductance converter (SEPIC) [1]. For convenient comparisons of current and voltages stresses as well as conduction losses fifteen active power factor correction topologies with non pulsed input current are presented [2]. A PWM boost rectifier circuit topologies is used for controlling a non isolated DC-rail voltage whilst drawing supply currents at a unity fundamental power factor and with a low total harmonic distortion [3]. Single-phase AC-to-DC rectifier with input power factor correction has many advantages, including fewer semiconductor components, simplified control, and high-performance features, and satisfies IEC 555 harmonic current standards [4]. The reduced conduction losses are obtained through the use of a single converter, instead of the conventional configuration, composed of a four-diode front-end rectifier followed by a boost converter [5]. A single-phase soft-switched boost AC-DC power-factor correction rectifier operates with fewer conduction losses and half the swing voltage stresses found in a standard boost converter [6]. Active power factor correction is to reduce the losses to a minimum without an increase of the costs [7]. Dual boost PFC (DBPFC) topology shows superior characteristics compared with traditional boost PFC [8]. A significant reduction in the conduction losses is achieved, since the circulating current for the soft switching flows only through the auxiliary circuit and a minimum number of switching devices are involved in the circulating current path, and the proposed rectifier uses a single converter instead of the conventional configuration composed of a four-diode front-end rectifier followed by a boost converter [9].

A bridgeless boost rectifier with low conduction losses and reduced diode reverse-recovery problems is used for power-factor correction. This boost rectifier can reduce the conduction losses and alleviate the diode reverse-recovery problems by using a coupled inductor and two additional diodes. Zero-current turn-off of the output diodes is achieved, and the reverse-recovery currents of the additional diodes are slowed down to reduce the diode reverse-recovery losses [10]. A novel zero-voltage-transition (ZVT) bridgeless power factor correction circuit (PFC) has an auxiliary circuit, consisting of a resonant inductor, two blocking diodes, one wheeling diode and an assist MOSFET, was used to reduce the turn-on switching loss of the two main switches of the bridgeless PFC circuit. Soft commutation of the main switches is achieved without imposing additional voltage stress on the main switches [11].

The PFC converter has incorporated a control method which drastically reduces the circulating power and hence raises the efficiency and completely eliminate any crossover distortion [12]. High efficiency can be obtained especially at low line condition because no input bridge rectifier is used. A concept of unique configuration of diodes has been used to reduce the common-mode (CM) conducted noise [13]. The” PFC power flow path of the proposed circuit has only two conduction drops in the current flow paths. Therefore, it can provide lower conduction loss [14]. A bridgeless dual-boost rectifier with reduced diode reverse-recovery problems is used for power-factor correction and conduction losses are lowered by essentially eliminating the full-bridge diode rectifier. The body diodes of the power switches are utilized as output diodes. Zero-current switching is realized when the body diodes are turned off [15].

An implementation of bridgeless PFC boost rectifier with low common-mode noise employs a unique multiple-winding, multi-core inductor to increase the utilization of the magnetic material [16]. In [17], a systematic review of the bridgeless PFC boost rectifier implementations that have received the most attention is presented along with their performance comparison with the conventional PFC boost rectifier. The bridgeless boost rectifier has the same major practical drawbacks as the conventional boost converter, such that the dc output voltage is always higher than the peak input voltage, input-output isolation cannot easily be implemented, the startup inrush current is high, and there is a lack of current limiting during overload conditions. Moreover, it is well known that the boost converter operating in discontinuous current mode (DCM) can offer a number of advantages such as inherent PFC function, very simple control, soft turn-on of the main switch, and reduced diode reversed-recovery losses. However, the DCM operation requires a high-quality boost inductor since it must switch extremely high peak ripple currents and voltages. As a result, a more robust input filter must be employed to suppress the high-frequency components of the pulsating input current, which increases the overall weight and cost of the rectifier. To overcome the drawbacks of a bridgeless PFC boost rectifier, two bridgeless topologies that are suitable for step-up/step down applications are introduced in [18] and [19]. However, the proposed topology in [18] still suffers from having three semiconductors in the current conduction path during each switching stage and it requires an isolated gate drive. On the other hand, the bridgeless topology presented in [19] has several advantages such as the presence of one or two semiconductors in the current conduction path and reduced voltage stress across the semiconductor devices; however, it also requires an isolated gate drive.
Single-ended primary-inductor converter (SEPIC) is a type of DC-DC converter allowing the electrical potential (voltage) at its output to be greater than, less than, or equal to that at its input; the output of the SEPIC is controlled by the duty cycle of the control transistor.

A SEPIC is similar to a traditional buck-boost converter, but has advantages of having non-inverted output (the output voltage is of the same polarity as the input voltage), the isolation between its input and output (provided by a capacitor in series), and true shutdown mode: when the switch is turned off, its output drops to 0 V. SEPICs are useful in applications in which a battery voltage can be above and below that of the regulator's intended output. For example, a single lithium ion battery typically discharges from 4.2 volts to 3 volts; if other components require 3.3 volts, then the SEPIC would be effective.

The schematic diagram for a basic SEPIC is shown in Figure 1. As with other switched mode power supplies (specifically DC-to-DC converters), the SEPIC exchanges energy between the capacitors and inductors in order to convert from one voltage to another. The amount of energy exchange is controlled by switch S1, which is typically a transistor such as a MOSFET; MOSFETs offer much higher input impedance and lower voltage drop than bipolar junction transistors (BJTs), and do not require biasing resistors (as MOSFET switching is controlled by differences in voltage rather than a current, as with BJTs).

**Continuous mode:** A SEPIC is said to be in continuous-conduction mode (or, continuous mode) if the current through the inductor L1 never falls to zero.

**Discontinuous mode:** A SEPIC is said to be in discontinuous-conduction mode (or, discontinuous mode) if the current through the inductor L1 is allowed to fall to zero.

During a SEPIC’s steady-state operation, the average voltage across capacitor C1 (V_C1) is equal to the input voltage (V_in). Because capacitor C1 blocks direct current (DC), the average current across it (I_C1) is zero, making inductor L2 the only source of load current. Therefore, the average current through inductor L2 (I_L2) is the same as the average load current and hence independent of the input voltage. Looking at average voltages, the following can be written: V_{IN} = V_{L1} + V_{C1} + V_{L2}

Because the average voltage of V_{C1} is equal to V_{IN}, V_{L1} = -V_{L2}. For this reason, the two inductors can be wound on the same core. Since the voltages are the same in magnitude, their effects of the mutual inductance will be zero, assuming the polarity of the windings is correct. Also, since the voltages are the same in magnitude, the ripple currents from the two inductors will be equal in magnitude. The average currents can be summed as follows: I_{D1} = I_{L1} - I_{L2}

When switch S1 is turned on, current I_{L1} increases and the current I_{L2} increases in the negative direction. (Mathematically, it decreases due to arrow direction.) The energy to increase the current I_{L1} comes from the input source. Since S1 is a short while closed, and the instantaneous voltage V_{C1} is approximately V_{IN}, the voltage V_{L2} is approximately -V_{IN}. Therefore, the capacitor C1 supplies the energy to increase the magnitude of the current in L2 and thus increase the energy stored in L2. The easiest way to visualize this is to consider the bias voltages of the circuit in a d.c. state, then close S1.

When switch S1 is turned off, the current I_{L1} becomes the same as the current I_{L2}, since inductors do not allow instantaneous changes in current. The current I_{L2} will continue in the negative direction, in fact it never reverses direction. It can be seen from the diagram that a negative I_{L2} will add to the current I_{L1} to increase the current delivered to the load. Using Kirchhoff’s Current Law, it can be shown that I_{D1} = I_{C1} - I_{L2}. It can then be concluded, that while S1 is off, power is delivered to the load from both L2 and L1. C1, however is being charged by L1 during this off cycle, and will in turn recharge L2 during the on cycle.
Because the potential (voltage) across capacitor C1 may reverse direction every cycle, a non-polarized capacitor should be used. However, a polarized tantalum or electrolytic capacitor may be used in some cases, because the potential (voltage) across capacitor C1 will not change unless the switch is closed long enough for a half cycle of resonance with inductor L2, and by this time the current in inductor L1 could be quite large.

The capacitor CIN is required to reduce the effects of the parasitic inductance and internal resistance of the power supply. The boost/buck capabilities of the SEPIC are possible because of capacitor C1 and inductor L2. Inductor L1 and switch S1 create a standard boost converter, which generate a voltage \( V_{S1} \) that is higher than \( V_{IN} \), whose magnitude is determined by the duty cycle of the switch S1. Since the average voltage across C1 is \( V_{DC} \), the output voltage \( V_O \) is \( V_{S1} - V_{IN} \). If \( V_{S1} \) is less than double \( V_{IN} \), then the output voltage will be less than the input voltage. If \( V_{S1} \) is greater than double \( V_{IN} \), then the output voltage will be greater than the input voltage.

II. PROPOSED BRIDGELESS RECTIFIERS

This proposes bridgeless PFC circuits based on SEPIC topologies with low conduction losses, as shown in Fig. 4. Unlike the boost converter, the SEPIC converters offer several advantages in PFC applications, such as easy implementation of transformer isolation, inherent inrush current limitation during start-up and overload conditions, lower input current ripple, and less electromagnetic interference (EMI) associated with the DCM topology [20]. Similar to the bridgeless boost presented in [5] and [7], the proposed topologies in Fig. 4 are formed by connecting two dc–dc SEPIC converters, one for each half-line period of the input voltage. The operational circuits during positive and negative half-line period for the proposed bridgeless SEPIC rectifier of Fig. 4 are shown in Fig. 3(a) and (b), respectively.

In our project, the ac input is converted into dc using two dc–dc sepic rectifiers. This sepic rectifier includes resonant LC circuit which produces high frequency pulses which is converted into dc by diode rectifier. The ripples in the output of the diode rectifier are eliminated by C filter. Now the non-pulsating voltage is obtained across the load.

Note that, by referring to Fig. 3, there are one or two semiconductor(s) in the current flowing path; hence, the conduction losses, as well as the thermal stresses on the semiconductor devices, are further reduced, and the circuit efficiency is improved compared to the conventional SEPIC rectifier. Moreover, Fig. 4 shows that the input ac line voltage is always connected to the output ground through the slow-recovery diodes \( D_p \) and \( D_n \). Thus, the proposed topologies do not suffer from the high common-mode EMI noise emission problem and has common mode EMI performance similar to the conventional topologies of Fig.1 Consequently, the proposed topologies appear to be promising candidates for commercial PFC products.
Each of the proposed rectifiers utilizes two power switches ($Q_1$ and $Q_2$), two low-recovery diodes ($D_p$ and $D_n$), and a fast diode ($D_o$). However, the two power switches can be driven by the same control signal, which significantly simplifies the control circuitry.

Moreover, the structure of the proposed topologies utilizes one additional inductor compared to the conventional topologies in Fig. 1, which are often described as a disadvantage in terms of size and cost. However, a better thermal performance can be achieved with the two inductors compared to a single inductor. On the other hand the three inductors in the proposed topologies can be coupled on the same magnetic core, allowing considerable size and cost reduction. Additionally, the “near-zero-ripple-current” condition at the input port of the rectifier can be achieved without compromising performance. This condition is very desirable, particularly for the DCM operation, because the generated EMI noise is minimized,
dramatically reducing input filtering requirements. Furthermore, the power component count in the proposed topologies is comparable to the conventional SEPIC PFC rectifiers in Fig. 1. Another advantage of the proposed rectifier is a reduction in the power switch current stress as compared to the conventional SEPIC PFC rectifiers. This is because each power switch is operating during half-line period. On the other hand, the components’ voltage stresses are equal to their counterparts in the conventional SEPIC converter. The remainder of this paper is organized as follows. The principle of operation is presented in Chapter III. Detailed analysis, modeling and comparisons are presented in Chapter IV. Simulation and experimental results are given in Chapter V, followed by conclusions in Chapter VI.

### III. PRINCIPLE OF OPERATION OF THE PROPOSED BRIDGELESS RECTIFIER

The proposed bridgeless rectifiers shown in Fig. 4 are constructed by connecting two dc–dc converters. Referring to Fig. 2, during the positive half-line cycle, the first dc–dc SEPIC circuit $L_1−Q_1−C_1−L_3−D_0$ is active through diode $D_p$, which connects the input ac source to the output ground. During the negative half-line cycle, the second dc–dc SEPIC circuit, $L_2−Q_2−C_2−L_3−D_0$, is active through diode $D_n$, which connects the input ac source to the output ground. Thus, due to the symmetry of the circuit, it is sufficient to analyze the circuit during the positive half-period of the input voltage. Moreover, the operation of the proposed rectifiers in Fig. 4 will be described assuming that the three inductors are operating in DCM. By operating the rectifier in DCM, several advantages can be gained. These advantages include the following: there is natural near-unity power factor, the power switches are turned on at zero current, and the output diode $D_o$ is turned off at zero current. Thus, the loss due to the turn-on switching losses and the reverse recovery of the output diode are considerably reduced.

Similar to the conventional SEPIC converters, the DCM for the proposed rectifier occurs when the current through diode $D_o$ drops to zero before the end of the switch off-time. Thus, the circuit operation during one switching period $T_s$ in a positive half-line period can be divided into three distinct operating modes, as shown in Fig.3(a)–(c), and it can be described as follows.

**STAGE 1:** Fig. 3(a) $Q_1$ on, $D_p$ forward biased, $D_o$ off

In this stage, the three-inductor currents linearly increase at a rate proportional to the input voltage $v_{ac}$. This interval ends when $Q_1$ is turned off, initiating the next subinterval.

**STAGE 2:** Fig. 3(b)

At the instant, switch $Q_1$ is turned off, diode $D_o$ is turned on, simultaneously providing a path for the three inductor currents. Diode $D_p$ remains conducting to provide a path for $i_{L1}$ and $i_{L2}$. In this stage, the three inductor currents linearly decrease at a rate proportional to the output voltage $V_o$. This interval ends when the output diode current $i_{Do}$ smoothly reaches to zero and $D_o$ becomes reverse biased.

**STAGE 3:** Fig. 3(c)

In this stage, both $Q_1$ and $D_o$ are in their off-state. Diode $D_p$ provides a path for $i_{L3}$. The three inductors behave as current sources, which keeps the currents constant. Hence, the voltage across the three inductors is zero. Capacitor $C_1$ is charging up by $i_{L1}$, while $C_2$ is discharged by $i_{L2}$. Fig. 5 shows the main theoretical waveforms during one switching period $T_s$. 

![Fig. 3(a) Q1 on, Dp forward biased, Do off](image)
Fig. 3(b) Q1 off, Dp on, Do on

Fig. 3(c) Q1 off, Dp off, Do off

The circuit operation during one switching period $T_s$ in a negative half-line period can be divided into three distinct operating modes, as shown in Fig. 3(d)–(f), and it can be described as follows:

**STAGE 1: Fig. 3(d)**
When the switch $Q_2$ is turned on, diode $D_n$ is forward biased by the sum inductor currents $i_{L1}$ and $i_{L2}$. As a result, diode $D_p$ is reversed biased by the input voltage. The output diode is reversed biased by the reverse voltage ($v_{ac} + V_o$). In this stage, the three-inductor currents linearly increase at a rate proportional to the input voltage $v_{ac}$. This interval ends when $Q_2$ is turned off, initiating the next subinterval.

**STAGE 2: Fig. 3(e)**
At the instant $Q_2$ is turned off, diode $D_o$ is turned on, simultaneously providing a path for the three inductor currents. Diode $D_n$ remains conducting to provide a path for $i_{L1}$ and $i_{L2}$. In this stage, the three inductor currents linearly decrease at a rate proportional to the output voltage $V_o$. This interval ends when the output diode current $i_{Do}$ smoothly reaches to zero and $D_o$ becomes reverse biased.

**STAGE 3: Fig. 3(f)**

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In this stage, both $Q_2$ and $D_0$ are in their off-state. Diode $D_n$ provides a path for $i_{L3}$. The three inductors behave as current sources, which keeps the currents constant. Hence, the voltage across the three inductors is zero. Capacitor $C_1$ is charging up by $i_{L1}$, while $C_2$ is discharged by $i_{L2}$.

![Fig.3(f) Q2 off, Dn on, D0 off](image)

It should be mentioned here that if the two active switches $Q_1$ and $Q_2$ are implemented as standard MOSFET, then the body diode of $Q_2$ will conduct during the first stage and the circuit will not properly function. In other words, there are reverse voltages applied to the active switches, so that the switches must have reverse blocking capability. Therefore, a unidirectional current conducting device must be implemented for $Q_1$ and $Q_2$. In this case, turning ON or OFF $Q_2$ during the first stage will not change the circuit operation mode. Accordingly, both switches $Q_1$ and $Q_2$ can be driven by the same control signal, which helps in reducing the cost and complexity of the driving circuit.

IV. ANALYSIS AND COMPARISON

A. Voltage Conversion Ratio
The voltage conversion ratio $M = V_o/V_m$ in terms of circuit parameters can be found by evaluating the average output diode current $I_{D0}$ during one line-cycle of the ac input voltage.

$$I_{D0} = \frac{1}{T} \int i_{D0} \, dt \quad \text{-------------------------- (1)}$$

where the average output diode current over one switching period $T_s$

The average output diode current over one switching period is given by

$$i_{D0} = D_2 \frac{T_s}{2L_e} v_0 \quad \text{--------------------- (2)}$$

Substituting (2) in (1) and evaluating (1) gives

$$I_{D0} = \frac{V_m}{2R_e} V_0$$

Where $R_e$ is the input resistance of the converter and equals

$$R_e = 2 \frac{L_e}{D_1} T_s$$

On the other hand, the average output diode current over one line cycle is equal to the average current through the load $R_L$, $i_0$. Thus, one can simply show that the desired voltage conversion ratio $M$ is equal to

$$M = \left[ \frac{R_L/2R_e}{2} \right]^{1/2} = \left[ \frac{D_1}{2K_e} \right]^{1/2} \quad \text{---------------- (3)}$$

$$K_e = 2 \frac{L_e}{R_L} T_s$$

The voltage conversion ratio $M$ in (3) is the same expression obtained for the conventional PFC sepic rectifier in DCM [20] expect for the definition of $L_e$

B. Input line current
Assuming that the efficiency is close to unity, the average input current over one switching period can be obtained from the instantaneous power balancing between the input and output ports of the rectifier: thus,

$$v_{ac} i_{ac} = v_0 \cdot i_{D0}$$

where $i_{ac}$ represents the input line current averaged during one switching cycle. By substituting (2) in (4), we obtain

$$i_{ac} = \frac{v_{ac}}{R_e} \quad \text{----------------- (5)}$$

Similar to the conventional sepic rectifier, (5) shows that the input port of the proposed rectifier obeys Ohm’s law so that the input current is sinusoidal and in phase with the input voltage.

C. Boundaries Between CCM and DCM
Referring to the output diode $D_0$ current waveform in DCM operation mode requires that the sum of the duty cycle and the normalized switch off-time length to be less than one, i.e.,

$$D_2 < 1-D_1 \quad \text{------------------------ (6)}$$
Substituting $D_2 = D_1 \sin(\omega t) / M$ into (6) and using (3), the following condition for DCM is obtained:

$$Ke < K_{e\text{-crit}} = \frac{1}{(2 M + \sin(\omega t))^2}$$

It is clear that from the above equation that the value of $Ke$ depends on the line angle $(\omega t)$. Hence the minimum and the maximum values of $K_{e\text{-crit}}$ are

$$K_{e\text{-crit-min}} = \frac{1}{2 (M + 1)^2}$$
$$K_{e\text{-crit-max}} = \frac{1}{2 (M)^2}$$

respectively. Therefore, for values of $Ke < K_{e\text{-crit-min}}$, the converter always operate in DCM, and it operates in continuous conduction mod (CCM) for values of $Ke > K_{e\text{-crit-max}}$. However, for the values of $K_{e\text{-crit-min}} < Ke < K_{e\text{-crit-max}}$ the converter operates in both the modes, i.e., in CCM near the peak value of the line voltage and in DCM near the zero crossing of the input line voltage.

D. Semiconductor Stresses

When operating a converter in the DCM region, the current stress on the converter components becomes relatively large compared to the CCM operation, and this leads to one disadvantage of the DCM operation which limits this operating mode to low-power applications (<300W). Table I shows the normalized voltage and current stresses across the semiconductor devices for the converter in Fig 2. Voltages and currents are normalized with respect to the peak input value $V_m$ and output load current ($V_o/R_L$).

E Comparison Between Conventional and Bridgeless Sepic PFC rectifier

The circuit components in both the conventional PFC sepic and the proposed bridgeless Sepic PFC rectifier have similar peak voltage and current stresses. However, the bridgeless Sepic subjects the input inductors (L1 and L2), the coupling capacitors (C1 and C2), and the active switches (Q1 and Q2) to a lower rms current stress compared to their counterparts in the conventional topology. Moreover, since the bridgeless Sepic is constructed by connecting two dc-dc converter, the switching performance of the two converters remains the same which results in similar switching losses. In contrast, as shown in table II the input current in the bridgeless Sepic flows through fewer power semiconductor devices compared to the conventional Sepic PFC.

<table>
<thead>
<tr>
<th>Devices</th>
<th>Peak voltage</th>
<th>Rms current</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1 and Q2</td>
<td>$1+M$</td>
<td>$\left[\frac{2D_1}{3K_e}\right]^{1/2}$</td>
</tr>
<tr>
<td>D0</td>
<td>$1+M$</td>
<td>$8\left[3(3)^{1/2}(2K_e)^{1/4}\right]$</td>
</tr>
<tr>
<td>Dp and Dn</td>
<td>$1$</td>
<td>$M$</td>
</tr>
</tbody>
</table>

V. SIMULATION RESULTS

![Fig. 5 (a) Circuit diagram](image)
<table>
<thead>
<tr>
<th>Item</th>
<th>Bridgeless Sepic</th>
<th>Conventional sepic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slow diode</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>Fast diode</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Switch</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

Current conduction path:
- **Stage 1**: 1 slow diode, 1 switch 2 slow diodes, 1 switch
- **Stage 2**: 1 slow diode, 1 fast diode 2 slow diodes, 1 fast diode
- **DCM**: 1 slow diode 2 slow diodes

![Fig. 5 (b) Input voltage and current waveforms](image)

![Fig. 5 (c) I_L1 current waveform](image)

![Fig 5 (d) I_L2 current waveform](image)

![Fig 5 (e) Vc1&Vc2 waveforms](image)
Fig 5 (f) $I_L$ current waveform

Fig. 5(g) Switching pulse waveform & Gate voltage and Drain to source voltage waveforms

Fig 5 (h) $I_D0$ Current flow through $D0$

Fig 5 (i) Output current waveform

Fig 5 (j) Output voltage waveform
VI. CONCLUSION

The new single-phase bridgeless rectifier with low input current distortion and low conduction losses has been presented and analysed. The proposed bridgeless rectifiers are derived from the conventional sepic converter. Comparing with conventional sepic circuit due to lower conduction loss and switching loss, the proposed topology can further improve the conversion efficiency. Namely, to maintain same efficiency, the proposed circuits could operate with higher switching frequency. Simulation results of the proposed bridgeless Sepic rectifier on a 65-W prototype at 48 V input voltage have been given to show high performance in terms of high power factor efficiency.

REFERENCES