Performance Evaluation of ECC in Single and Multi Processor Architectures on FPGA Based Embedded System

Sruti Agarwal1,∗, Sangeet Saha2, Rourab Paul3, Amlan Chakrabarti4

1Institute of RadioPhysics and Electronics, University of Calcutta, Kolkata.
2CSE, University of Calcutta, Kolkata.
3A. K. Choudhury School of I.T., University of Calcutta, Kolkata.
4Senior Member IEEE, A.K. Choudhury School of I.T., University of Calcutta, Kolkata.
e-mail: shruti5u@gmail.com

Abstract. Cryptographic algorithms are computationally costly and the challenge is more if we need to execute them in resource constrained embedded systems. Field Programmable Gate Arrays (FPGAs) having programmable logic devices and processing cores, have proven to be highly feasible implementation platforms for embedded systems providing lesser design time and reconfigurability. Design parameters like throughput, resource utilization and power requirements are the key issues. The popular Elliptic Curve Cryptography (ECC), which is superior over other public-key crypto-systems like RSA in many ways, such as providing greater security for a smaller key size, is chosen in this work and the possibilities of its implementation in FPGA based embedded systems for both single and dual processor core architectures involving task parallelization have been explored. This exploration, which is first of its kind considering the other existing works, is a needed activity for evaluating the best possible architectural environment for ECC implementation on FPGA (Virtex4 XC4VFX12, FF668, -10) based embedded platform.

Keywords: dual-core, ECC, FPGA, MicroBlaze, shared memory, single-core.

1. Introduction

ECC is an approach to public-key cryptography based on the algebraic structure of elliptic curves over finite fields. The use of elliptic curves in cryptography was suggested independently by Neal Koblitz [1] and Victor S. Miller [2] in 1985. Elliptic curve cryptography, in essence, entails using the group of points on an elliptic curve as the underlying number system for public key cryptography. The primary reason for using elliptic curves as a basis for public key crypto-systems is that elliptic curve based crypto-systems appear to provide better security than traditional crypto-systems for a given key size [4], thereby reducing the process overhead. One can take advantage of this fact to increase security, or (more often) to increase performance by reducing the key size while keeping the same security.

Designers are now working on designing dedicated hardware accelerator blocks along with the main processor [5,7,8] to increase the throughput of the design. ECC algorithm is used for secured communication in smart cards [9] and also in GSM security [6]. So, high speed, resource constrained environment is required. Using a dual-core instead of a dedicated co-processor enables the user to operate from the application layer without entering the subordinate layers. Also, the thread-level parallelism, used by the dual-core ensures higher throughput without increasing the much power, which is an important issue for low-power communication devices like smart cards. Implementations can be made in different platforms namely, FPGA or ASIC or can be done using micro-controllers. FPGAs provides reconfigurability and lesser design time, while ASIC provides better throughput though the design time is large and expensive. We propose the design and implementation of Elliptic Curve Cryptography (ECC) encryption algorithm by developing suitable single core and dual core design on Xilinx Virtex 4 (ML403) device. The system is optimized in terms of execution speed. We perform a trade-off between throughput, power and resource requirements for our dual core implementation. To the best of our knowledge, dual-soft core processor based implementation of ECC in an FPGA is not yet available in related literatures and hence it is first of its kind.

The paper is organized as follows: Section 2 details the overview of ECC, the encryption and decryption process. The design and implementation details for single and dual-core processor architectures are described in Section 3. The experimental results are summarized in Section 4. Conclusion and References are briefed in Section 5.

2. Background

This section provides some background on elliptic curves and ECC and then the hardness of decrypting the elliptic curve ciphers is also discussed. The idea of a multi processor system, establishment of communication between the processors using shared memory and the needed data synchronization is also briefed in the later part of this section.

2.1 Elliptic curves

Elliptic curves are described by curves, which are similar to cubic equations, used for calculating the circumference of an ellipse. In general, cubic equations for elliptic curves take the following form known as Weierstrass equation [3]:

\[
(y^2 + axy + by) \mod p = (x^3 + cx^2 + dx + e) \mod p \tag{1}
\]

where \(a, b, c, d, e, p\) are real numbers and \(x, y\) take on any values in the real numbers. For our purpose, it is sufficient to limit ourselves to equation of the form given in Equation 2 for appropriate curve parameters of ECC.

\[
y^2 \mod p = (x^3 + ax + b) \mod p \tag{2}
\]

Figure 1 shows an example of elliptic curve.
2.2 Elliptic curve cryptography

ECC can be used to encrypt a plain text message \( M \) into cipher text for secured communication. Firstly, the plain text message \( M \) is converted into a set of finite points \( P_M(x, y) \), which lie in the elliptic curve \( E_p(a, b) \). A generator point, \( G \in E_p(a, b) \), is chosen next such that the smallest value of \( n \) for which \( nG = O \) is a very large prime number. The elliptic curve \( E_p(a, b) \) and the generator point \( G \) are then made public.

Let there be two parties \( A \) and \( B \) who wish to communicate using ECC. Each user selects a private key, user \( A \)'s private key is \( n_A \), while \( n_B \) is the private key for user \( B \) such that \( n_A, n_B \) are very large prime numbers. Then they compute their public keys. The public key of \( A \) is \( P_A = n_AG \), while for \( B \) the public key is \( P_B = n_BG \). To send the secret message to \( B \), \( A \) encrypts the message point \( P_M \) by choosing a random number \( k \) and computes the cipher text points \( C_M \) using \( B \)'s public key. The cipher text is given by:

\[
C_M = [(kG), (P_M + kP_B)]
\]

(3)

On receiving the cipher text (pair of points) \( C_M \), \( B \) multiplies the first pair of points \( (kG) \) with his private key \( n_B \), and then adds the result to the second point of the cipher text \( (P_M + kP_B) \) i.e.,

\[
(P_M + kP_B) - [n_B(kG)] = (P_M + kn_BG) - [n_B(kG)] = P_M
\]

(4)

Plain text message point \( P_M \), corresponds to the message \( M \). It is to be observed here that only \( B \) can remove \( n_B(kG) \) from the second part of the cipher text. No, third party or intruder can know the message except \( B \). Thus, ECC is very secured and can be relied for confidential communication. Breaking of ECC is a “hard problem”, which requires computing of discreet logarithm [3].

2.3 Multi processor system

A multi processor system consists of two or more processors working concurrently and capable of communicating with each other. Such a design tends to double the throughput, with two processors
running independently, but with an extra cost of resource and power. On the other hand, a multi core system is one in which more than one processor is build on the same die. In FPGA we have on-chip soft processor cores, which has been utilized in our design to multi core design. There are some basic conditions required for the execution of a design in a multi core system. The primary being concurrency in the design i.e., no data dependency must be present in processes that run in different processors and also the two processors must have some handshaking for synchronization of data. Multi core processors often use a shared memory system or a Mailbox system as an interprocessor communication mechanism, that operates very quickly [11].

2.4 Shared memory

In a multi core environment, mailbox and shared memory [12] are the two mechanisms, provided by Xilinx. Out of these two mechanisms, shared memory is the most common and most intuitive way of passing information between processing subsystems and we have used it in our design.

A shared memory system has the following properties [12]:

- Any processor can refer any location in the shared memory directly by some system call.
- Location of data in memory is transparent to the programmer. Data could be distributed across multiple processors, with the help of some proper API, data can be handled at program level.
- A synchronization is a must for accessing the shared memory segment by some hardware/software protocol between the two processors.

Shared memory is typically the fastest asynchronous mode of communication, especially when the information to be shared is large. Shared memory gives another approach of “in-place” message processing schemes. Shared memory can be built out of on-chip local memory like BRAM or on external memory like DDR SDRAM.

2.5 Synchronization

The region in which the shared data is stored is known as a Critical Region in operating system terminology. Unless there is some sort of well-defined non-conflicting way in which each processor accesses the shared data, the multi core system cannot work properly. A synchronization protocol or construct is usually required to serialize accesses to the shared resource.

The XPS Mutex synchronization primitive is used in this work, which is provided by Xilinx as a separate IP-core [13]. When using Shared memory as a method of data communication, the pseudo code should look like this to ensure proper synchronization,

```c
/* shared tasks */
XMutex_Lock();
/* Critical Region – Perform shared memory access */
XMutex_Unlock();
```

By calling the `XMutex_Lock()` it must be ensured that one processor is accessing the critical region and other processor should not be allowed to access the same until `XMutex_Lock()` is called by that processor.
3. Design and Implementation

This section highlights the key components of our proposed design. At first, we describe the processor that is used and then we brief the design innovations made to enhance the throughput.

3.1 MicroBlaze

The MicroBlaze embedded processor soft core is a 32-bit Reduced Instruction Set Computer (RISC) optimized for implementation in FPGAs [10]. As a soft-core processor, MicroBlaze is implemented entirely in the general-purpose memory and logic fabric of Xilinx FPGAs. The Embedded Development Kit (EDK) platform from Xilinx has been used to build a complete processor system on FPGA.

3.2 ECC in single MicroBlaze

In a single processor architecture, the FPGA receives the input via the RS-232 port through UART and then the input plaintext message is encrypted using ECC algorithm, which is running in the MicroBlaze processor of the the FPGA. After encryption, the cipher text is send back to the Host PC and is seen in the Hyper Terminal using serial communication between the board and the PC. Figure 2 shows the flow of steps in the design. Processor working at 100 MHz clock frequency is used to encrypt 8-bits of message using ECC. Scalar multiplication constitutes the main operation in ECC. It is seen that the processor takes 19.01 msec to perform the total encryption. The resource utilized i.e., the number of LUTs and slices required by the design as well as the power requirements are summarized in the Table 2.
3.3 ECC in Dual MicroBlaze

After evaluating the performance of ECC in single processor architecture by using MicroBlaze soft-core processor, another approach is taken to implement it in Dual processor architecture by considering the fact discussed in Section 2.3 for higher throughput and efficiency. Xilinx Virtex4 ML403 is taken as a platform for design. Shared memory is used for creating a handshaking between the two processors as described in Section 2.4 and the synchronization for communication is achieved using the process described in Section 2.5.

Figure 3 shows the architecture of Dual MicroBlaze design.

In addition, multiple port memory controller (DDR−SDRAM) and inter-processor communication-XPS Mutex hardware IP [13] is also incorporated in the test bed to facilitate the memory sharing and inter processor synchronization and communication.

In the experiment, the two processors are equally engaged to execute ECC in parallel fashion and in between the consequent steps, the two processors communicate with each other via shared memory with proper synchronization. The message to be encrypted is transferred to the FPGA from a computer using RS232 serial port communication. The two multiplications are executed concurrently in two processors and the resulting data is assembled in the shared memory. The addition operation is then performed by the 1st processor and the resultant cipher text is generated. The resultant cipher text is send back to the PC using the RS232 interface and is viewed at the Hyper Terminal of the computer. Figure 4 shows the mechanism in which the two processors communicate using the shared memory and using Mutex locking and unlocking.

4. Result and Analysis

It is seen that the encryption engine speeds up by 3.3 times as the proposed architecture takes only 5.72 msec to perform the encryption. The resource estimation, power required and throughput
measurements for both the designs are shown in Table 1 and 2 below. The design improves the throughput of execution, but utilizes more resources due to the dual cores. It is to be noted here that the throughput of the design can be improved further by enabling the cache memory. But due to the resource constraints of our implementation board the cache memory of the two processors could not be enabled.

Table 1. For an encryption process.

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Clock Freq. (in MHz)</th>
<th># Clock Cycles Req'd.</th>
<th>Time Reqd. (in msec)</th>
<th>Throughput (bits per sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-core Microblaze</td>
<td>100</td>
<td>1901317</td>
<td>19.01</td>
<td>420.83</td>
</tr>
<tr>
<td>Dual-core Microblaze</td>
<td>100</td>
<td>572552</td>
<td>5.72</td>
<td>1398.60</td>
</tr>
</tbody>
</table>

Table 2. Resource and power estimation for the encryption process.

<table>
<thead>
<tr>
<th>Processor</th>
<th>Clock Freq. (in MHz)</th>
<th># Slices</th>
<th># Slice FFs</th>
<th># 4-Input LUTs</th>
<th>Throughput per slice</th>
<th>Total Power (in Watts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-core Microblaze</td>
<td>100</td>
<td>3580</td>
<td>3750</td>
<td>4076</td>
<td>0.1175</td>
<td>1.106</td>
</tr>
<tr>
<td>Dual-core Microblaze</td>
<td>100</td>
<td>5313</td>
<td>6637</td>
<td>7495</td>
<td>0.2632</td>
<td>1.808</td>
</tr>
</tbody>
</table>
5. Conclusion and Future Work

This work is an exploration of ECC implementation for FPGA based embedded systems. Two specific designs have been addressed, the first one is simpler involving a single Microblaze core whereas the other one utilizes two Microblaze cores and thus enables multi-threading. The dual core based implementation gives almost a 3 times increase in the throughput but utilizes almost twice the resource and 30\% more power as compared to the single core based implementation. This clearly shows a trade off between speed, resource utilization and power requirement. In future we look forward to do a further exploration of ECC implementation for embedded applications involving FPGA based hard processor cores and ASIC based design.

References