Simulation Results of a Low-Drift Integrator for Aditya Tokamak

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Abstract

In Aditya tokamak, the accurate knowledge of the position of the plasma boundary is essential in order to maintain a safe distance between plasma and in vessel component. This requires calculation of magnetic field topology which can be done by integrators. The proposed simulated method uses a new integrator system which is composed of integrator module and instrumentation amplifier module. Psice software has been used for the simulation. This integrator system gives an improved output when compared with a conventional analog integrator. The drift produced by input offset voltage and bias current has been successfully eliminated by the proposed method.

Keywords: Amplifier, drift, integrator, offset, Plasma

1. Introduction

TOKAMAK (Toroidal chamber with magnetic coil) is a name of a nuclear fusion device which is having poloidal and toroidal magnetic field. In this device these magnetic fields are used to confine a plasma, which is the fourth state of matter. since, no solid material could withstand the extremely high temperature of the plasma. The discharge of plasma produces a continuous pulse (long pulse) which can be taken outside the boundary of tokamak with the help of magnetic pick up loops. The signal from the loop has to be integrated to find the local magnetic field, magnetic flux and plasma current. High accuracy integrators are required for the accurate measurement of steady state long pulses. It is really a big challenge to build a high accuracy integrator, since the integrators are subjected to intrinsic difficulties. Integration drift and saturation of the integrator are the two difficulties while designing an integrator.(i) Integration drift: It is due to offset and temperature induced drift of the amplifier, noise etc. (ii) Saturation of the integrator:

The saturation of the integrator occurs in the case of high flux variation such as disruption. The integration drift and saturation effect increases with time, which introduces an absolute error and also limits the integration working duration at a certain specified accuracy.

The new integrator has to be designed for the requirements of long pulse integration. Fig.1 shows the general block diagram of the long pulse integrator. The system should have the integral module, signal conditioning module and error correcting module. The output signal of the integrator will be transmitted directly to the plasma control system (PCS) for the plasma equilibrium and shape control, and to the data acquisition system (DAS) for the physical analysis. The following examples are the methods of designing an integrator for various Tokamak devices

S.Ali Arshad and L.de kock [1] developed an analog integrator for International Thermonuclear Experimental Reactor (ITER). In this method pair of integrators is used, one initially A, connected to the source (eg.magnetic probe) and the other, initially B, to a resistor via a set of switches. The integrator system could be accurate to within a few millivoltseconds, with no special temperature control of the environment.

Pascal Spuig et.al., [2] also developed an analog integrator which is used on Tore Supra. It is based on a differential input structure principle with two frontal integration cells. Each integration cell is based on an analog operational integrator with an offset correction implemented by a dynamic auto-compensation feedback.

J. Strait et.al., [3] developed the digital–analog integrator for DIII-D tokamak. It utilizes a passive RC integrator followed by an amplifier, analog-to-digital convertor (ADC), and real-time digital signal processor (DSP). In this method, the RC time constant is long compared to the ADC sampling interval Δt, but short

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D. M. Liu, et.al., [5] developed a new low drift integrator for EAST. The systematic diagram of the integrator system is mainly composed of the integral module and the Ethernet control module. The integral module integrates the input signals and regulates the output signals [6].

2. Proposed Methodology

In the proposed method operational amplifiers has been used for the construction of the integrators. The op-amp has input offset voltage (Vios) and the input bias current (Ib). In the absence of input voltage or at zero frequency (d.c), op-amp gain is very high. The input offset voltage gets amplified and appears at the output as an error voltage. The bias current also results in a capacitor charging current and adds its effect in an output error voltage. The two components, due to high dc gain of op-amp cause output to ramp up or down depending upon the polarities of offset voltage/bias current. After sometime, output of op-amp may achieve its saturation level. Hence, there is possibility of op-amp saturation due to such an error voltage and it is very difficult to pull op-amp out of saturation. These difficulties are eliminated in the proposed methodology.

This system is mainly composed of an integrator module and an amplifier module. The integral module used for actual integration and the amplifier module used for drift reduction and amplification. The circuit diagram of an integrator system is shown in fig.2

2.1. Integrator module:

It has two integrators namely integrator1 and integrator2. In order to calculate the correct drift value, the same type of integrators should be selected. Both inputs of integrator1 are grounded and the inverting terminal of integrator2 is connected to the test input signal. The output of the integrators1 and 2 is equal to Vo1 and Vo2 which is given by

\[
Vo1 = \frac{-1}{RC} \int (V_{ios1} - V_{os1}) dt
\]

(1)

\[
Vo2 = \frac{-1}{RC} \int (V_{in}(t) + R_{ios2} - V_{os2}) dt
\]

(2)

Where \(V_{in}(t)\) is the input signal, \(I_{os1}\) and \(I_{os2}\) are the input offset currents of integrator1 and 2 and \(V_{os1}\) and \(V_{os2}\) are the input offset voltages of integrator1 and 2.
The output of the integrator2 gives the actual integration of the test signal and the output of integrator1 is taken as reference for calculating offset induced drift in an integrator. Hence the two integrators should be selected with same characteristics, so that the input offset drift also being same. It has been minimized easily with the help of instrumentation amplifier.

2.2 Instrumentation amplifier:

In this method, a three op-amp instrumentation amplifier is used (from fig.3). It is composed of two stages. The op-amp A3 and A4 are the non-inverting amplifiers forming the input stage. The op-amp A5 is the normal difference amplifier forming an output stage of the amplifier. Vo1 and Vo2 are the input from the integrator module to the op-amps A3 and A4. The output of the instrumentation amplifier is taken from the op-amp5, which is given by,

$$ V_o = \frac{R_2}{R_1} (V_{o4} - V_{o3}) \quad (3) $$

Where Vo3 and Vo4 are the outputs of op-amp A3 and A4. Which is given to the inputs of A5. The instrumentation amplifier used in the proposed method for drift reduction. For example, an integrator circuit using op-amp op-07 is tested without input signal is shown in fig.3. From the figure it has been noted that for 10 s the offset voltage of -0.14v. It has been further drift downwards with respect to time. Up to 120 s the response of integrator without input signal has been noted. After some duration the offset voltage has been saturated and reaches a dc supply voltage of an op-amp. Since offset voltage affect the overall performance of the integrator, this offset induced drift and saturation effect has to be minimized by the proposed method. Hence, in the proposed method an instrumentation amplifier has been utilized in order to eliminate the error. In this system it is actually used as a difference amplifier which subtracts the offset error value of the integrator and produces a drift free output signal.

3. Result And Discussion

The integrator system is simulated using Pspeice software and the corresponding output is shown in fig 4.

Reference signal test: The square wave input signal of 3V amplitude, 100 Hz frequency and the positive and negative half period of 10 ms time period has been tested in the i. It has an integration time constant of 20 ms, and the output should be triangular waveform with a peak amplitude is given by

$$ V_{o2} = V_{in} \frac{T}{2RC} = 3(10ms)/2(20ms) = 750mv. $$

This output signal can be amplified and the offset errors can be eliminated with the help of instrumentation amplifier. The output from the instrumentation amplifier with the gain value of 5 is given by the following expression

$$ V_o = (1+2R_f/R_g)(V_{o2} - V_{o1}) = 3.75V. $$

The square wave input of different amplitude has been tested and the corresponding outputs are tabulated in table 1. Hence, it is noted that the input offset voltage and bias current errors are eliminated in this method by subtracting the output of integrator1 by integrator2. This can be done with the help of instrumentation amplifier. This method gives improved result when compared with the conventional analog integrators. The fig.5 shows the output of the conventional analog integrator. In this integrator the same square wave signal is tested and the output signal is having amplitude only 450mv (instead of 750mv).

<table>
<thead>
<tr>
<th>INPUT SIGNAL FREQUENCY</th>
<th>INTEGRATOR OUTPUT</th>
<th>AMPLIFIER OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>500Hz</td>
<td>140mv</td>
<td>0.7v</td>
</tr>
<tr>
<td>1KHz</td>
<td>80mv</td>
<td>0.36v</td>
</tr>
<tr>
<td>2KHz</td>
<td>40mv</td>
<td>0.18v</td>
</tr>
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</table>

Table 1 - Tabulation For Different Square Wave Frequencies

References

Fig. 4. Input and output waveform of conventional integrator

Fig. 5. Input and output waveform of proposed integrator