Routing Aware Scan Re-Ordering for Minimizing the Power

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Abstract— Scan DFT is a standard post silicon debugging technique for digital design. The scan design is most widely used structured DFT technique. It increases the controllability and observability for flip flops. As industry moving towards submicron technology scan power becoming very important. The main sources of power dissipation are shifting power and capturing power. If shifting power and capture power crosses the chips threshold power limit, it can lead to burnout of the chip. So it is necessary to minimize the power to over safe chip testing. There are different ways to minimize the scan power, out of them RTL level and layout level scan power minimization techniques are most popular. The techniques that are applied at RTL level may leads to congestion, on routable problem in the latest stage of the ASIC design flow. So post layout scan power minimization technique can be a good methodology to bring the trade-off between layout congestion and scan power. This paper concentrates on minimizing the test power at layout level. Once it has a scan flip flop position at the layout level, it will try to identify which flops needs to be re-order with respect to the given test patterns to minimize the scan power. These are the two algorithms implemented; Scan Re-Ordering For Minimizing the Power, Scan Re-Ordering For Minimizing the Routing Congestion.

Index Terms— DFT, Scan design, Low Power, X-Filling techniques, Scan re-ordering.

I. INTRODUCTION
Testing VLSI circuit bridges the gap between the imperfection of the manufacturing process for integrated circuits (IC) and the end user’s expectations of defect-free chips. Manufacturers test their products to discard the faulty components to ensure that only the defect-free chips make their way to the consumer. With the advent of deep sub-micron technology, the tight constraints on power dissipation of VLSI circuits have created new challenges for testing low power VLSI circuits which need to overcome the traditional test techniques that do not account for power dissipation during test application.

The scan design has been a widely used DFT technique which can guarantee high fault coverage for a complex design by enhancing its controllability and observability [1]. When using the scan design to shift test data, however, a large number of signal transitions may occur along the scan paths, which induces even...
more signal transitions on the circuit-under-test (CUT). Therefore, with the scan design, the CUT will consume much more power in its test mode than that in its functional mode. This excessive power consumption during the scan-based testing may result in physical damage or reliability degradation to the CUT, and in turn decreases the yield and product lifetime [2]. As the number of scan cells keeps on growing in modern designs, this increasing power consumption has become one of the biggest barriers to effective the scan-based testing.

A common method to lower the power consumption during scan-based testing is to reduce the number signal transitions of scan cells, which can be classified into the following three types: (1) the capture transition – generated by the same scan cell’s value difference between the scan-in pattern and the corresponding captured response, (2) the scan-out transition – generated by two adjacent scan cells’ value difference between their scan-out response, and (3) the scan-in transition– generated by two adjacent scan cells value difference between the scan-in patterns. The first transition type is associated with the capture power and the last two types are associated with the scan-shift power.


E. Alpaslan, Y. Huang, X. Lin, W.-T. Cheng, and J. Dworak, —Reducing scan shift power at RTL, in Proc. VLSI Test Symp., 2008, pp. 139–146, this paper describe how to reduce shift power at RTL level. But power minimization technique at RTL level leads routing congestion at layout level [3].

Methods are proposed to utilize the don’t-care bits to minimize the scan-in transitions for a given test set [4][5][6][7]. [4] Proposed don’t-care-filling technique, named MT-fill, guaranteeing that the scan-in transitions generated by its filled patterns are minimized for the given test set. The methods in [4][5][6] reduced the test power as well as the test data volume based on building-compression hardware. [7] Added Xor gates or inverters along the scan paths to minimize the scan-in transitions. However, none of [4][5][6][7] considered the scan-out transitions simultaneously.

Methods in [8][9][10][11] change the order of scan cells along the scan paths to minimize both scan-in and scan-out transitions based on given test patterns and responses. This scan-cell reordering technique saves the scan-shift power, but sacrifices the opportunity of optimizing the wire length of scan paths during the place and route stage. So this project is focusing on routing congestion along with power.

II. MOTIVATION

Personal mobile communications and portable computing systems are the fastest growing sectors of the consumer electronics market. The electronic devices at the heart of such products need to dissipate low power, in order to conserve battery life and meet packaging reliability constraints. During the scan-based testing, the total power consumption of the DUT is highly correlated with the total number of signal transitions on the scan cells [4]. In this paper, we use the number of signal transitions on scan cells as the power model of the whole DUT. The proposed scan-cell-reordering algorithm focuses on reducing the total scan-shift power, i.e., reducing the total scan-shift transitions. The capture power is not considered in the proposed algorithm.

From the discussions in part I, the scan-in transitions can be minimized by wisely filling the don’t-care bits of a test set once the scan-cell order in the scan paths are given [4]. This reduction could be more significant as the percentage of don’t-care bits increases. Therefore, our scan-cell reordering algorithm attempts to first minimize the scan-out transition count without specifying the don’t-care bits, leaving the don’t-care bits for a later minimization of scan-in transition, such as MT-fill [4]. However, before specifying the don’t-care bits, the value of some responses may not be obtainable, implying that no explicit information of scan-out transitions can be used during the scan-cell reordering process.

The other algorithm implemented uses either MT-fill or re-ordering scan cells; using re-ordering scan cells power reduces by little extent and using MT-fill power dissipation reduces more compared to re-ordering scan cells. Also there is a routing congestion problem in re-ordering scan cells. In order to avoid power dissipation (more compared to previous methods) and routing congestion problems, the new algorithm—Routing Aware Scan Re-ordering for minimizing the powerl is implemented.
III. PROBLEM STATEMENT AND ANALYSIS

A. Problem Statement

As industry moving towards submicron technology scan power becoming very important. The main sources of power dissipation are shifting power and capturing power. If shifting power and capture power crosses the chips threshold power limit, it can lead to burnout of the chip. So it is necessary to minimize the power to over safe chip testing. For a given design (sequential circuit in Verilog netlist form), generate a set of test patterns and reorder the flip-flops in the scan chain, so that power dissipation becomes minimum. Power can be estimated by computing the number of signal transitions occurring in the various lines of the circuit.

B. Terminologies and Analysis

In this context it is necessary to define the metrics of power consumption of a digital circuit. These concerns involve energy, average power, instantaneous power and peak power.

1. Energy: Which is the total switching activity occurred during test pattern application and also called shift power. By this battery lifetime will be reduced.

2. Average Power: The total distribution of power over a time period. High average power adds to the thermal load and it should be vented away from the device under test.

3. Instantaneous Power: The value of power consumed at any given instant.

4. Peak Power: The highest value of power at any given instant. The peak power determines the thermal and electrical limits of components.

The objective of this project is to optimize the total power or energy consumption. Generally, power consumption is more in the test mode than in the normal mode due to following reasons.

- Test circuitry embedded into a design under test (DUT) to reduce test complexity. This test circuit is idle during the normal operations, but used extensively in the test mode.
- The test efficiency shows a high correlation with the toggle rate.
- In a circuit, parallel testing frequently used to reduce application time.

All the above factors contribute in the elevated power dissipation in the circuit. Essentially, the energy consumption of a circuit would be decreased if it is possible to minimize the toggle rate.

IV. ASSUMPTION AND OBJECTIVES

In this project it is assumed that the circuit is given and also assumes that there is a single scan chain in the circuit. As there exists a high correlation between the switching activities in the internal nodes of the circuit with transitions taking place in scan cells. It is further assumed that the primary inputs are directly controllable and all the switching activities in the circuit are due to transitions in the scan cells. These project objectives are as follows.

1) To generate test patterns with X-cubes.
2) Filling of X's with either 0 or 1 such that the total power consumptions due to toggling is minimized by using X-filling Algorithm (MT-fill algorithm).
3) To determine the order of the scan cells such that the total power consumption due to toggling is minimized.
4) To determine the order of the scan cells such that the total length of scan chain is minimized.

V. PROJECT FLOW

The project description involves the detailed illustration of the various stages involved in the project. The main algorithms are

- Scan Re-Ordering For Minimizing the Power
- Scan Re-Ordering For Minimizing the Routing Congestion

In addition to above algorithms this project also discussing X-filling Techniques, random fill algorithm and MT fill algorithm and also power calculation using weighted transition count (WTC).

C. Scan Re-Ordering For Minimizing the Power: The Figure 1 shows Design Flow for Scan Re-Ordering Looking into Power

1) RTL Synthesis
Figure 1: Design Flow for Scan Re-Ordering Looking into Power

The process of reducing the RTL to the gate-level netlist is called synthesis. This project is using Synopsys’s Design Compiler for RTL synthesis. Design Compiler tool takes a RTL hardware description, and standard cell library as input and the resulting output would be a technology dependent gate-level-netlist. The gate-level-netlist is nothing but structural representation of only standard cells based on the cells in the standard cell library.

2) Scan Insertion and Stitching
As IC’s become increasingly more difficult to test through conventional functional vectors, IC engineers start to design test structures into digital circuits to help ease the burden of testing. This concept of making circuits more testable is called Design-for-Testability. The major contributor to the complexity of the functional test vectors is the existence of flip flops and pipeline stages. However this issue can be resolved if the flip flops can be made directly controllable and observable. This idea is realized through scan insertion by using Mentor Graphic’s DFT Advisor tool for inserting and stitching of scan cells.

3) Test Pattern Generation
Mentor Graphic’s FastScan tool is used for generating test patterns. The scanned netlist and ATPG setup files got from DFT Advisor are used as inputs to FastScan.

The following list describes the basic process for using FastScan:

- FastScan require a structural (gate-level) design netlist and a DFT library. At invocation, the tool first reads in the library and then the netlist, parsing and checking each. If the tool encounters an error during this process, it issues a message and terminates invocation.
- After a successful invocation, the tool goes into Setup mode. Within Setup mode, you perform several tasks, using commands either interactively or through the use of a dofile. Within Setup mode, you can also specify information that influences simulation model creation during the design flattening phase.
- After performing all the desired setup, you can exit the Setup mode. Exiting Setup mode triggers a number of operations. If this is the first attempt to exit Setup mode, the tool creates a flattened design model. This model may already exist if a previous attempt to exit Setup mode failed or you used the Flatten Model command.
- Next, the tool performs extensive learning analysis on this model.
- Once the tool creates a flattened model and learns its behaviour, it begins design rules checking.
- Once the design passes rules checking, the tool enters either Good, Fault, or Atpg mode. While typically you would enter the ATPG mode, you may want to perform good machine simulation on a pattern set for the design.
- You may also just want to fault simulate a set of external patterns.
- At this point, you may typically want to create patterns. However, you must perform some
additional setup steps, such as creating the fault list. You can then run ATPG on the fault list. During the ATPG run, the tool also performs fault simulation to verify that the generated patterns detect the targeted faults.

4) Scan Re-Ordering Algorithm Looking Into Power

Before discussing scan re-ordering algorithm, X-filling techniques and method to calculate weighted transition count (WTC) are discussing. The X-filling techniques discussing here are random fill technique and dynamic MT-fill technique. Figure 2 shows method to calculate weighted transition count.

Consider input vector V1=0101, WTC (V1) =1*1+1*2+1*3=6 and for response vector R1=0001, WTC (R1) =0*3+0*2+1*1=1. Similarly for V3, WTC (V3) =1*1+0*2+1*3=4 and for R3, WTC (R3) =1*3+1*2+0*1=5.

The equation 1 is used for calculating weighted transition count:

\[ WTC = \sum (n - btp_i) / \text{other terms} \]

Where n is the number of scan flip-flops and btp_i is the bit transition position at i^th position and i vary from 1 to n-1. If no bit transition in vector then consider btp_i=0.

D. Scan Re-Ordering For Minimizing the Routing Congestion: The Figure 3 shows Design Flow for Scan Re-Ordering Looking into Routing Congestion. The following are the stages in design flow

- RTL Synthesis
- Scan Insertion and Stitching
- Test Pattern Generation
- Place and Route
- Scan Re-Ordering Algorithm Looking Into Routing Congestion

1) RTL Synthesis: RTL Synthesis process is already explained in previous section.
2) Scan Insertion and Stitching: Scan Insertion and Stitching process is already explained in section.
3) Test Pattern Generation: Test Pattern Generation is already explained in section.
4) Place and Route: After getting scanned netlist from DFTAdvisor flow, go for place and route. As the name suggests, the layout tool performs the placement and routing. The placement tool starts the physical implementation of the ASIC. When ASIC designer provides 2-D floorplan, the placer tool assigns locations for each gate in the netlist. The resulting placed gates netlist contains the physical location of standard-cells, but retains an abstract description of how the gates' terminals are wired to each other. Typically the standard cells have a constant size in at least one dimension that allows them to be lined up in rows on the integrated circuit.

The chip will consist of a huge number of rows (with power and ground running next to each row) with each row filled with the various cells making up the actual design. Placers obey certain rules: Each gate is assigned a unique (exclusive) location on the die map. A given gate is placed once, and may not occupy or overlap the location of any other gate.

The quality of floorplan and placement is more critical than the actual routing. Optimal cell placement location, not only speeds up the final routing, but also produces superior results in terms of timing and
reduced congestion. Using the placed-gates netlist and the layout view of the library, the router adds both signal connect lines and power supply lines. The fully routed physical netlist contains the listing of gates from synthesis, the placement of each gate from placement, and the drawn interconnects from routing.

**Figure 3: Design Flow for Scan Re-Ordering Looking Into Routing Congestion**

5) Scan Re-Ordering Algorithm Looking Into Routing Congestion: After the placement of cells, the clock tree is inserted in the design is called clock tree synthesis. Once CTS is over routing is performed by the tool and finally chip finishing is done. Finally we will have scan cells information in DEF file. The test patterns generated without don’t care bits from FastScan and scan cells information in DEF file from IC Compiler (place and route) are inputs to the algorithm. The DEF file has information of all cells, but we need only scan cells information. This algorithm reads DEF file and extract scan cell positions (co-ordinates). The extracted scan cells information is stored in data structure, is used to calculate routing length between each pair of scan cells. The equation 1 is used to calculate routing length between scan cells.

\[ D_{ij} = |x_i - y_i| + |x_j - y_j| \]

Equation 2 is called Man Hatten Distance formula. And also calculate weighted transition count before scan cell re-ordering. Next re-order scan cells using heuristic algorithm such that total routing length is minimum. Now Calculate weighted transition count after scan re-ordering.

VI. RESULTS

A. Results of Scan Re-Ordering Algorithm Looking Into Power

The Table I shows, Results of Scan Re-Ordering Algorithm Looking into Power. The result shows that the power is minimized after scan re-ordering. Here algorithm takes test patterns without don’t care bits, so necessary of use of x-filling technique. Hence test coverage is 100%.

B. Results of Scan Re-Ordering Algorithm Looking Into Routing Congestion

The Table II shows, the results of Scan Re-Ordering Algorithm Looking into Routing Congestion. From this Table, it shows that routing congestion is minimized after scan re-ordering and also power is minimized.

VII. CONCLUSIONS

The dynamic power dissipation due to switching activities in scan cells is main source of power dissipation.
### Table I: Results of Scan Re-Ordering Algorithm Looking Into Power

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Test Coverage (%)</th>
<th>#Patterns</th>
<th>Total Weighted Transition Count Before Scan Re-Ordering</th>
<th>Power Reduction in Percentage</th>
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<td>100</td>
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<td>13207984</td>
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<td>S5495</td>
<td>100</td>
<td>23</td>
<td>2942</td>
<td>16.64</td>
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</tbody>
</table>

### Table II: Results of Scan Re-Ordering Algorithm Looking Into Routing Congestion

<table>
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<tr>
<th>Circuit</th>
<th>Test Coverage (%)</th>
<th>#Patterns</th>
<th>Total Routing Congestion Before Scan Re-Ordering</th>
<th>Routing Congestion Reduction in Percentage</th>
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In order to minimize the dynamic power dissipation, this project used scan re-ordering algorithm. In addition to scan re-ordering algorithm, x-filling techniques are used to minimize more power, for these test patterns are generated with don’t care bits. The re-ordering of scan cells may lead to routing congestion, so this project also implemented routing aware scan cell re-ordering, for this scan cell positions are required. The scan cells information got from place and route.

The results in Table 1, shows that power is minimized after scan re-ordering. If x-filling techniques adopted with scan re-ordering algorithm then power is minimized at maximum rate (60% for design s13207). The Table 2 shows that the routing congestion is minimized after scan re-ordering and also power is minimized. The scan design with single scan chain is used in this project work, this can require more clock cycles for shifting test pattern into scan chain. If number of scan cells increases then clock cycles required for shifting patterns also increase. Hence in future work by making multiple scan chains minimize the test application time.

In addition to multiple scan chains use clock gating to minimize clock cycles. Also this project implemented scan re-ordering algorithm looking into routing congestion, which minimizes power dissipation due to routing length is more but power minimization due to switching activity is less. Hence in future works consider trade off between these two; this will be done considering both weighted transition count and routing length.

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