BIST based Pattern Generation for Low Power VLSI Architecture

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Abstract—In the semiconductor manufacturing industry recently remarkable technological developments like, feasibility of millions of transistors and various other components to be integrated on a Chip with enormous packaging options, several designing procedures and proficient test methods have contributed massively in the integration of the entire system on a chip. A revolution in the approach to designing and testing an IC is in trend However, the testing industry has a higher-end of challenges [2]. The introduction of the Built-In Self-Test architecture has been a giant leap in the testing industry. The role of the BIST circuit is to reduce the cost by reducing the testing interval and the complexity of testing. The power dissipated in a circuit during testing mode is considerably larger than that dissipated in the operational mode. This increase in power dissipated can be ascribed to the decreased correlation existing between the random patterns generated in the test mode [1]. Hence, the idea behind this thesis is to design a DFT circuit that will help in decreasing the switching activities in the test mode in order to limit the power dissipation and at the same time obtain the mandated fault coverage ratio. This directly relates to the decrease in the cost of the circuitry.

Index Terms—Built-In Self-Test, VLSI Testing, LFSR technique, low-power test vector pattern generation.

I. INTRODUCTION

Today’s System-On-Chip (SOC) devices contain integration of a large number of processors, different types of memories like SRAM, user defined logic and Digital signal processors, with an increasing count in transistors on a single chip thereby, challenging the design and testing methodologies in vogue [1]. The testing of ICs, today, mandates a new and high-level of competence and accuracy, expecting complete verification through all of the stages of the design process. It is known fact that power dissipation in the circuit during the test mode is significant compared to that in the normal mode. This can be attributed to the correlation existing between consecutive test vectors applied during the normal mode of operation of the circuit. However, this is not the case in the test mode. There is no considerable correlation between consecutive vectors in the test mode. This automatically means that the primary switching activities will be more in the test mode compared to that in the normal mode and that the power dissipation will be higher in the test mode. Thus, more the transitions between the tests vectors more will be the power dissipated. Hence, low power testing is the need of the hour.

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One way of solving this issue by use of Built-In-Self-Test (BIST) design. A BIST circuitry is contained as a part of the target system that aids in the verification of the internal functionalities of the particular circuit it is assigned. BIST is a methodology of allowing test logic to be incorporated as a part of the chip itself. The BIST architecture is widely accepted because of its very many advantages like the reduction in test application time, reduction in the cost of generation of test vectors, to allow at-speed testing, to provide an alternative to the expensive Automatic Testing Equipment (ATE) and the reduction in the volume of test data. Also, the overhead area occupied by the BIST in the circuit can be considered negligible in comparison to the size of the target system [2]. The BIST makes the target system independent of any external automatic equipment for testing [1].

Hence, this proposed method aims to analyze and discuss a circuit that generates test patterns that help reduce the average and peak power dissipation in BIST architecture during testing mode. Also, efforts are made about to bring appropriate modifications to the logical and structural implementation, of the circuit under consideration, in order to reduce the power dissipation even further.

II. TEST PATTERN GENERATION

Test patterns are basically a set of inputs (1’s and 0’s) which, when applied in a circuit, will determine if the circuit is working as per the requirement or if it is faulty.

2.1 Need for low power testing

The System-On-Chips platform imposes a challenge in the design and testing methodology. Testing gains the primary significance in terms of issues and expenditure, thereby, demanding a wide range of possible novelties. The area of concentration, here, is power dissipation [1]. In general, the power consumed during the test mode is more than that in the normal mode of operation. This additional power dissipated may pose a threat to the circuitry and can also lead to a breakdown of the chip. This in turns will raise the costs, increase the difficulty in verifying the performance of the circuit and thereby reduce the final code [1]. Having learnt the above, the necessity of decreasing the power dissipated in a circuit during the test mode is a major milestone for further advancements in VLSI design.

A number of reasons can be quoted for the increased power consumption in the circuit during the test mode [2]. Decreased correlation between the test vectors can be sited as the first reason. Normally, a considerable correlation exists between the inputs during the operational mode but may not be the same in the test mode. This decreased correlation in the input during the test mode increases the switching activities, thereby increasing the power dissipation [1]. Secondly, the use of parallel testing process by test engineers in order to reduce the test application time can result in increased power dissipation. The third reason can be attributed to the DFT circuit that is inbuilt in the design for the test mode, which normally idled during the operational mode, however, is extensively active in the test mode [2].

III. LOW POWER MODELS UNDER CONSIDERATION

3.1 The modelled low power test pattern generator

The primary task in the designing of a BIST circuit is in ensuring low power dissipation during the test mode by reducing the primary switching activities. Here, the low power test pattern generator named LP-TPG adopted in [1] is discussed as an example. Two consecutive random test vectors generated from an LFSR is taken as the base. Considering the base patterns, the circuit is accordingly modeled so as to generate three intermediate test vectors in between the two consecutive random test vectors generated from the LFSR. This introduction of the intermediary vectors helps in reduction of the average power and the peak power since the number of transitions between the two base patterns from the LFSR and number of transitions between the two base patterns including the three patterns inserted from the new model is the same. This directly relates to the minimized power consumption in the new model than that in the conventional LFSR and implies that the correlation between the test vectors generated by LP-TPG is more than the correlation between the conventional LFSR vectors. This technique also takes into deliberation that the randomness of the generated patterns is not reduced.

The two consecutive random test vectors generated by the conventional LFSR are named $P_i$ and $P_{i+1}$, were in $P_i = \{P_{i1}, P_{i2},..., P_{in}\}$ and $P_{i+1} = \{P_{i+11}, P_{i+12},..., P_{i+1n}\}$. Here, $n$ represents the number of transistors that are switched for every clock pulse and are generated as bits at the output. This determines the switching activity of the circuit under test. The three intermediary patterns generated by the introduction of the new Low Power model are named $P_{k1}$, $P_{k2}$ and $P_{k3}$.  

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Referring to Figure 1, we observe that Pk2 is generated as the intermediary of Pi and Pi+1, i.e., The first half of Pi and the second half of Pi+1 is combined to form Pk2. 

Here, Pk2 is again a random vector because it is obtained from two random vectors only. Once Pk2 is obtained, the bits of Pi and Pk2 are compared to generate Pk1. If a particular bit of Pi is equal to the corresponding bit of Pk2, then the corresponding bit of Pk1 is represented by that particular bit. For example, in the 1st bit position, both Pi and Pk2 have bit ‘1’, hence, bit ‘1’ is represented as the 1st bit position for vector Pk1 as well. However, if they are not equal, then the corresponding bit of Pk1 is substituted by R (which is ‘0’) as shown below in this case.

\[ t_{j}^{k1} = \begin{cases} t_{j}^{i} & \text{if } t_{j}^{i} = t_{j}^{k2} \\ R & \text{if } t_{j}^{i} \neq t_{j}^{k2} \end{cases} \]

Where \( j \in \{1, 2, \ldots, n\} \). Similarly, Pk3 is generated by the comparison of Pk2 and Pi+1. This method of generating the vectors Pk1 and Pk3 is called R-Injection. Here, we observe that the number of switching activities between the vectors Ti and Ti+1 is equal to the sum of switching activities between the & Pk1, Pk1 & Pk2, Pk2 & Pk3 and Pk3 & Pi+1. This is represented as below.

\[
\sum_{j=1}^{n} t_{j}^{i} - t_{j}^{i+1} + \sum_{j=1}^{n} t_{j}^{k1} - t_{j}^{k2} + \sum_{j=1}^{n} t_{j}^{k2} - t_{j}^{k3} + \sum_{j=1}^{n} t_{j}^{k3} - t_{j}^{i} = \sum_{j=1}^{n} t_{j}^{i} - t_{j}^{i+1}
\]

However, the point to be considered in this place is that the test time, on the whole, and the fault coverage remains the same with the introduction of the intermediary test vectors.
Above referred is the LP-TPG designed, by integrating the proposed logic with the conventional LFSR, to generate the three intermediary patterns. The circuit consists of an 8-bit external-XOR LFSR with polynomial $x^8 + x + 1$ and seed = 01001011. Each time the values of first four flip flops are shifted to the right according to the signals the shaded flip holds the value of the 4th flip-flop.

R-Injection circuit - The R-Injection circuit consists of an AND gate, an OR gate and a 2*1 multiplexer. The R-Injection circuit holds the current state and the next state of the corresponding bits of each vector. When both the corresponding bits are equal, the AND and the OR gate generates the same value of the bit. However, when the corresponding bits are not equal, the random bit R is given to the output.

Multiplexer - As is known, it consists of two AND gates and an OR gate. The inputs to one of the AND gates are sel signal and the output of the corresponding R-Injection circuit. The other AND gate gets its inputs as sel BAR and the output of the corresponding flip-flop. The output of the AND gate is then ORed to give the final output.

The random vectors are generated with the help of two enable signals (en1 & en2) and to select signals (sel1 & sel2) and is not dependent on the size or the polynomial of the LFSR. Signal Sel1 is connected to the first four multiplexers, and signal Sel2 is connected to the last four multiplexers. The Sel signal selects either the output of the LFSR or the output of the R-Injection circuit accordingly. If Sel = ‘1’, then the LFSR outputs are provided to the output and if Sel = ‘0’, then the R-Injection circuit’s outputs are available at the final output. Similarly, signal en1 is connected to the first four flip-flops, and en2 is connected to the last four flip-flops. If en = ‘1’, then the respective half of the flip flops to which the en signal is connected are active and the values pertaining to those flip flops are shifted to the right. However, if en = ‘0’, the half of the flip flops to which the signal is connected is in the idle mode and do not shift their values to the right. The circuit also consists of the clock and the Test_en signal that uses the select the Test mode. This circuit generates vectors as are shown and described next.

### Table I. An Example of LP-TPG Using an 8-Bit LFSR

<table>
<thead>
<tr>
<th>clk</th>
<th>Pattern</th>
<th>en1 en2</th>
<th>sel1 sel2</th>
<th>LP-LFSR</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$P^1$</td>
<td>1 0 1 1</td>
<td>1 1 0 1</td>
<td>1 0 1 0 1</td>
</tr>
<tr>
<td>2</td>
<td>$P^{k1}$</td>
<td>0 0 1 0</td>
<td>1 0 1</td>
<td>1 0 1 0 1</td>
</tr>
<tr>
<td>3</td>
<td>$P^{k2}$</td>
<td>0 1 1 1</td>
<td>1 0 0</td>
<td>1 0 0 1 1</td>
</tr>
<tr>
<td>4</td>
<td>$P^{k3}$</td>
<td>0 0 0 1</td>
<td>1 1 1</td>
<td>1 1 1 0 1</td>
</tr>
<tr>
<td>5</td>
<td>$P^2$</td>
<td>1 0 1 1</td>
<td>0 1 0</td>
<td>0 1 0 1 0</td>
</tr>
</tbody>
</table>

**Step 1:** sel1 sel2 = 11, en1 en2 = 10.
When sel1 sel2 = 11, it means that the multiplexer is designed to select the outputs of the LFSR for both halves of the LFSR circuitry. Similarly, When en1 en2 = 10, it means that the first half of the LFSR is active, but the second half is in the idle mode. On this command, the vector $P^1$ is generated.

**Step 2:** sel1 sel2 = 10, en1 en2 = 00.
When sel1 sel2 = 10, the first half of the LFSR output and the second half of the R-Injection circuit are given to the final outputs. Similarly when en1 en2 = 00, both halves of the LFSR are idle and do not shift values for that clock pulse. These signals are generated vector $P^{k1}$.

**Step 3:** sel1 sel2 = 11, en1 en2 = 10.
In this case when sel1 sel2 = 11, both halves of the LFSR are obtained at the final output and the second half of the LFSR is in the idle mode, whereas the first half of the LFSR is active for en1 en2 = 10 and the bits are shifted to the right. In this case, the values of the four flip flops are shifted to the shaded flip flop. Once this process if completed, the vector $P^2$ is generated.

**Step 4:** sel1 sel2 = 01, en1 en2 = 00.
When sel1 sel2 = 01, then second half of the LFSR outputs and the first half of the R-Injection circuit’s outputs are available on the main output, and When the signal en1 en1 = 00 are enabled, both halves of the flip flops are in the idle mode. Vector $P^{k3}$ is generated for this procedure.
Step 5: The procedure as in step 1 is repeated here and vector $T_{i+1}$ is generated. The above method continues from step 1 through step 5 for as many clock cycles as is required. The complete circuit is controlled by a finite state machine (FSM), as is shown in the below circuit that acts as the gear stick in the generation of the test patterns. The FSM serves as the control unit for the generation of the test patterns by continuing through steps 1 to 4. The inputs to the FSM are test_en and clk. When test_en = 1, the FSM is initiated with step 1 wherein en1 en2 = 10 and sel1 sel2 = 11 and continues till step 4 with the generation of a vector for every clock pulse. As can be observed, the intermediary vectors $P_{k1}$, $P_{k2}$ and $P_{k3}$ are generated between two consecutive random vectors $P_1$ and $P_2$. It is seen that the number of transitions between $P_1$ and $P_2$ are 7. However, the transitions between $P_1$ & $P_{k1} = 1$, $P_{k1}$ & $P_{k2} = 2$, $P_{k2}$ and $P_{k3} = 2$ and that between $P_{k3}$ and $P_2 = 2$. This shows that the switching activities between the test vectors, after the introduction of the three intermediary vectors, has significantly reduced, between the patterns, thereby reducing the average and peak power dissipation.

IV. MODIFIED LOW POWER TEST PATTERN GENERATOR

Three approaches aimed at reducing power consumption have been analyzed and discussed in this section. All of these approaches are concentrated on modifying the behavioural model of the LP-TPG under consideration. In the original circuit, the R-Injection circuit is responsible for introducing a random bit if the corresponding bit position has different values. In order to achieve this, the R-Injection circuit consists of an AND gate, and OR gate and a 2*1 multiplexer as mentioned in figure 4. The R-Injection circuit takes the current input and output values of D-fl of the LFSR circuit as input. These bits are ANDed and ORed inside the R-inject circuit. Hence the output of AND gate holds high value when both current input and output value of D-fl are high. While OR gate holds high value when either current input or output of D-fl is high. Then the outputs of AND and OR gates are inputted to a 2:1 MUX, whose select pin (R) is inputted by the main circuit. In the circuit, the select input randomly assigns either first or second input of the MUX to it’s output pin. The status of the select pin of the MUX is entirely depended on the status of output of D-fl which holds the MSB of the generated pattern.

![Figure 3. The modelled low power LFSR (LP-TPG)](image_url)

![Figure 4. R- Injection circuit](image_url)
A. Approach 1
In this approach, the complications of the R-Injection circuit containing the Multiplexer are removed. The R-inject circuit contains a simple 2-input AND gate which is inputted by the current input and output values of the respective D-ff as shown in figure 5. The AND gate holds high at its output when both current input and output are high. Here, bit ‘1’ is injected as random bit when the current and the next status of a flip flop are high, and bit ‘0’ is injected as a random bit if either the current or the next status of a flip flop or both are low. It also reduces the bulkiness of the R-inject circuit with less power to operate.

![Figure 5. 2 input AND gate](image)

B. Approach 2
In this approach, the R-inject circuit consists an OR gate as shown in figure 6. This OR gate is inputted by the current input and output values of the respective D-ff. The OR gate holds high at its output when either current input or output or both are high. Here, bit ‘0’ is injected as random bit, when either the current or future or both statuses of a flop is low and bit ‘1’ is injected as random bit if both the current and the next status of the flip-flop is high. Even here the bulkiness of the R-inject circuit is reduced with less power to operate.

![Figure 6. 2 input OR gate](image)

C. Approach 3
We have observed that several patterns have repeatedly generated by the original circuit (fig 4). Every repeated pattern does not contribute to the fault coverage. Instead, it may cause more transition in the CUT (Circuit Under Test), which intern results in more dynamic power loss. This unnecessarily increases the weighted switching activity (WSA). In order to overcome this issue, we propose a new approach by extending the original circuit as shown in the figure 8. Here, the overall circuit is split into 3 parts blocks.
The First block generates the low power patterns as explained in 3.1 sections.
The Second block captures all generated pattern by the first block. This block extracts all repeated pattern. Then it sorts all non-repeated patterns either in ascending or descending order. This approach reduces the unnecessary switching activity due to repeated patterns.
The third block will apply the non-repeated and sorted patterns into the CUT.

V. RESULTS
A. Simulation of the LFSR and the LP-TPG
The below snapshot provides the simulation results of the standard LFSR and the Low Power - Test Pattern Generator. As discussed earlier, 256 patterns are considered pertaining to an 8-bit vector. Also, the assumption is made that each transition consumes 1 watt of power for the calculations to be made simpler. The simulation calculates the total amount of transitions and the peak power for the number of vectors generated. It also separately provides details of the average and peak power of the said 256 patterns. The total number of transitions for the LFSR is 3343 whereas the total number of transitions for the LP-TPG is 1367. It is observed that there is a reduction of 60% of transitions in the LP-TPG compared to that of the LFSR. In the case of the Average power, it is 5.36078W for the LP-TPG and 13.1098W in the case of the
LFSR, which means there is a reduction of 60% of reduction in the average power. The Peak power is 30W for the LFSR and 21W for the LP-TPG. This confirms a reduction in peak power of about 30%. The weighted switching activity for the LP-TPG is calculated as 0.591086.

B. Simulation of the modified LP-TPG – Approach 1
The simulation results of the modified approach 1 are given. Here, we notice that the total numbers of transitions for the modified model are 1506. We obtained 1367 for the LP-TPG. It is observed that the average is 5.90588 in this approach but, only 5.36078 for the LP-TPG and this give an increase in the average power by 10.16% in comparison to the LP-TPG. However, the Peak power of this model is 19, whereas it was 21 for LP-TPG. Hence, the Peak power has been reduced by 10%.

C. Simulation of the modified LP-TPG – Approach 2

Below give are the simulation results of the modified approach 2. The total numbers of transitions for this approach are 1449. It was 1367 for the LP-TPG. Also, the average power is 5.68235 in this approach. It is a little lower than Approach 1. The average power for LP-TPG is 5.36078. Thus, the average power has increased by 5.9% in comparison to the LP-TPG. The Peak power for the LP-TPG and this model are 21 and 19 respectively. The Peak power is similar to that obtained in Approach 1, however the average power has been reduced further. Also, the weighted switching activity for this approach has been calculated to be 0.566557.

D. Simulation of the modified LP-TPG – Approach 3

Approach 3 produces simulation results as shown in the snapshot below. We observe a considerable decrease in the total amount of transitions; it is 789 compared to 1367 for the LP-TPG. The average power of this approach and the LP-TPG are 3.09412 and 5.36078W respectively. This is a decrease of 42.28% compared to the LP-TPG and is a significant reduction. The peak power of this model is 25, whereas, it is 21 for the LP-TPG. This describes that the peak power of this model is 19.04% more than the LP-TPG. However, since the Average power is considered more important for a circuit than the Peak power, Approach 3 is considered the best of the three approaches shown in table 2.

VI. ANALYSIS AND DISCUSSION

6.1 Power consumption of LFSR Pattern Generator
6.2 Power consumption of LP-TPG Pattern Generator
6.3 Power consumption of the modified LP-TPG Pattern Generator
TABLE II. COMPRESSION RESULT

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Bench Mark Circuit : Full Adder</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>LFSR</td>
</tr>
<tr>
<td>Count</td>
<td>3343</td>
</tr>
<tr>
<td>Average Power</td>
<td>13.10 W</td>
</tr>
<tr>
<td>Peak Power</td>
<td>30 W</td>
</tr>
</tbody>
</table>

VII. SUMMARY AND CONCLUSIONS

With reference to the reviews and examples of the several BIST circuits discussed, it is clearly noted that the power dissipated during the test mode can be limited by various methods. The fact that increasing integration leads to increased testing difficulties is the challenge that needs to be addressed. The experimental results of this project must reflect the decrease in the average and peak power without any reduction in the fault coverage ratio.

REFERENCES


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