A Novel 32 X 32 Low Power MAC Unit for Digital Hearing Aid Applications

V Anandi¹, Dr R Rangarajan², M Ramesh³ and R. Nithya⁴

¹ MSRIT/ECE.Bangalore,India
Email: anandi.v@msrit.edu

² Indus Engineering College/ECE,Coimbatore,India
Email: {profrr@gmail.com,ramandsur@gmail.com,nithya.rr@gmail.com}

Abstract—The ultra low power requirements of emerging implantable and wearable biomedical devices, necessitates, novel power management schemes. Multiplier is one of the critical components in applications in the area of digital signal processing, data encryption and low-power hearing aids. In this paper, efficient hardware architecture of MAC using a modified Wallace tree multiplier is proposed and validated. The proposed MAC uses multiplier with novel compressor designs and adders as primitive building blocks for fast low-power application. The partial products reduction block is completely redesigned using the novel compressors and the addition module is implemented using a new less complex full adder based on XNOR. The final adder is implemented using RCA. The resulting MAC is implemented in standard CMOS cell technology and compared both qualitatively and quantitatively with the existing hardware implementations. The experimental results show that the proposed implementation is faster and consume less power than similar hardware implementations making it a viable option for efficient designs. The 32x32 bit MAC unit designed using proposed full adder as the basic building block gave a power saving of 24.27% over 32 bit MAC designed using SERF full adder and 35.07% power savings over 32 bit MAC designed using conventional 28T full adder.

Index Terms—adder block, SERF full adder, compressor, low power MAC

I. INTRODUCTION

The increasing demand for portable systems and the need to limit power consumption and heat dissipation in very-high density chips have led to rapid developments in low-power design during the recent times. The battery lifetime is also a concern on the overall power consumption of the portable system. Hence, reducing the power dissipation of integrated circuits through design improvements is a major challenge in portable systems design. The need for low-power design is also an issue in high-performance digital systems, like microprocessors, digital signal processors (DSPs) and other applications. DSP is an important technology for many applications fields such as telecommunications, consumer electronics, disk drives, and navigation. Most of the DSP processors share a common feature designed to support fast execution of the repetitive computations of digital signal processing algorithms. A single-cycle MAC operation is useful in algorithms that involve computation in digital filters which are the main components of digital hearing aids. To achieve a single-cycle MAC, all DSP processors include a multiplier and accumulator as central elements of their data-paths. Real-time signal processing requires high speed and high throughput MAC unit that consumes low power, for a high performance digital signal processing system.

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A. Elements of a digital hearing aid

In order to meet the small size and ultra-low power requirements of hearing aids, the existing solutions resort to custom ASIC devices for each hearing aid design. This increases the final cost of the hearing aid to five times the cost of conventional analog hearing aids, which has limited the spread of these digital instruments.

By changing to a commercially available programmable DSP approach, the hearing aid companies could significantly reduce their costs, thereby reaching a larger portion of the population with a lower price, better sound quality digital instrument. The basic operations performed by a hearing aid are amplification, filtering, and output limiting. Various adaptive signal processing algorithms are being used to enhance the speech quality of the hearing aids. An adaptive filter is a filter that adjusts its transfer function according to an optimizing algorithm. For a large number of lattice filter stages, the longest delay can be reduced by a lattice filter optimization for speed which defers the final carry propagating addition until after the final lattice filter stage. The multiplication process is speeded up using booth multiplier and the accumulation process is done faster using the Wallace multiplier.[29]. A novel MAC unit employing column compression is proposed which can be integrated into a ultra low power DSP system for bio medical applications like digital hearing aids for improving the speed of spectral sharpening of speech enhancement and noise reduction algorithms.

B. Overview of Power Consumption in CMOS digital circuits

The average power consumption in conventional CMOS digital circuits can be expressed as the sum of three main components, namely, (1) the dynamic power consumption, (2) the shortcircuit power consumption, and (3) the leakage power consumption. If the system includes circuits like nonconventional CMOS gates that have continuous current paths between the power supply and the ground, static power component should also be considered.

\[ P_{\text{avg}} = P_{\text{switching}} + P_{\text{sc}} + P_{\text{leakage}} + P_{\text{static}} \]

C. Power Dissipation In Multipliers

The basic MAC Unit is made up of a multiplier and an accumulator. The multiplier can also be divided into the partial products generator, summation tree, and final adder. The summation network represents the core of the MAC unit. This block occupies most of the area and consumes most of the circuit power and delay. The addition network reduces the number of partial products into two operands representing a sum and a carry. The final adder is then used to generate the multiplication result out of these two operands. The last block is the accumulator, which is required to perform a double precision addition operation between the multiplication result and the accumulated operand. [3]. Multipliers are often found in the critical path of signal processors and are large block of a computing system.[2], [3].The amount of circuitry involved is proportional to the square of its resolution. The multiplier is a high delay block, and also a major source of power dissipation. Energy efficient parallel multiplier design requires analysis of multi application algorithms, technology constraints and circuit implementation techniques. In terms of power dissipation, the tree-based structure consumes lower power than the array-based structure [23].

D. Low Power Multiplier Structures

The most efficient multiplier structure will vary depending on the throughput requirement of the application. The serial multiplier implements the multiplication in \(n\) cycles for an \(n\times n\)-bit multipliers with least hardware [5]. The \(n\times n\)-bit serial multiplier requires a \(2n\) bit adders and shift registers to implement the multiplication. The parallel multipliers require more hardware compared to the serial multiplier in order to provide performance improvements. The parallel multipliers consist of three main computational blocks namely partial product generation, partial product reduction and final addition. After the partial product generation block, the partial products will be reduced to two rows, a row of sum and a row of carry signals. The final step is the addition of the generated carry and sum signals. [9]. A comparison of different multiplication algorithms in Ref. [3] has revealed that for the operands equal to or greater than 16-b, tree architecture based on encoding techniques such as Booth algorithm and in Ref. [4] Wallace provide higher performance with lower power dissipation than that of the array multiplier based on Baugh-Wooley or Braun algorithms [5].
For medium-bit operands (8-bit), the tree architecture multipliers are not power efficient and array architecture multipliers are not fast enough. Therefore, for an 8-bit multiplier a proper structure requires regularity of the array architecture and speed of tree architectures. The accumulation of the PPs, is performed using Reduction by rows (adders) and reduction by columns (counters). A direct method in the reduction by rows is to use multiple two-operand carry propagate adders (CPAs). Carry-save adders (CSAs) are efficient operators when three or more operands are to be added without propagating carries. A row of full-adders can be viewed as a mechanism to reduce three numbers to two numbers. An RCA turns into a CSA if carries are saved rather than propagated. A single bit full adder can be considered as a counter of 1’s at the input bits which can count three logical 1’s. [13].

**E. Low power adder types**

There are many different adder cells are introduced in literature like, XOR and transmission gate [1], pseudo-NMOS, Transmission gate CMOS, complementary CMOS, complementary pass-transistors [5] and XOR and pass transistor logic, SERF full adder [28], [29] with low number of transistors. The SERF Full adder is as shown in Fig. 4 [29], which does not operate reliably and is confronted with serious voltage drop problems especially at lower power supply voltages.
A new Full adder cell modified from SERF full adder has been designed using 24 transistors. The proposed cell has the advantage of low power consumption and high operating speed. The small transistor count leads to smaller silicon area. The proposed Low power Full adder is based on the static energy recovery concept [27], [28] and uses the Novel XNOR circuit and the Transmission Gate based MUX along with level restoring signal gating technique for its operation. By using signal gating Technique in Ref. [29], Ref. [30], the Carry out signal strength can be restored and reduce the power dissipation. The Sum is generated from the output of the second stage XNOR circuit, Sum = (A XNOR B) XNOR Cin. The Cout is calculated by multiplexing A & Cin controlled by (A ⊕ B). Compressors and 32 x 32 MAC unit are implemented using the proposed full adder. The 32x32 MAC is designed using 16x16 multipliers based on modified Wallace tree structure, with the addition of accumulator register at the final stage. [15], [16]. Compressors are mostly used in multipliers in the partial products summation stage to reduce the operands while adding the output terms of partial products [6],[7]. These Parallel counters have multiple-inputs, and multiple-outputs combinational logic circuits that determine the number of logic ONE’s in their inputs vectors and generate a binary coded output vector. Based on property of counter, a 15-4 compressor is constructed using eleven full adders. [19].

G. Results And Analysis
Six adder cells existing in literature are compared with the proposed adder for power, delay. (TABLE I) High speed compressors and multipliers using modified Wallace tree with the proposed full adder component were simulated and analyzed for their performance and functionality. Approximately 400 input patterns are applied to the multiplier to verify its functionality. Simulation results using CADENCE SPECTRE show that our multiplier can operate at 100 MHz in 0.18 µ CMOS technology under the supply voltage of 1.8 V. The power, delay, power delay product (PDP) values recorded for these designs. (Table II). Various multiply and accumulate (MAC) units were designed (8bit MAC, 16bit MAC and 32bit MAC) using the proposed full adder as the basic building module. The 32 bit MAC designed using proposed full adder, is compared against
32 bit MAC units designed, using conventional 28T full adder as its basic building block and using SERF full adder as its basic building block for performance. (Table III).

**TABLE I. FULL ADDER COMPARISON**

<table>
<thead>
<tr>
<th>Full Adder Designs</th>
<th>Power in uW</th>
<th>Delay in pS</th>
<th>PDP in fJ</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS 28T FA</td>
<td>46.43</td>
<td>208.70</td>
<td>9.6914</td>
</tr>
<tr>
<td>Optimized TG FA</td>
<td>46.91</td>
<td>51.46</td>
<td>2.4142</td>
</tr>
<tr>
<td>SERF FA</td>
<td>39.12</td>
<td>39.02</td>
<td>1.5264</td>
</tr>
<tr>
<td>Proposed FA</td>
<td>31.70</td>
<td>39.65</td>
<td>1.2570</td>
</tr>
</tbody>
</table>

**TABLE II. COMPRESSOR COMPARISON**

<table>
<thead>
<tr>
<th>Compressors</th>
<th>Power in uW</th>
<th>Delay in pS</th>
<th>PDP in fJ</th>
<th>EDP (10^-24J-sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4:3 Compressor</td>
<td>28.16</td>
<td>464.7</td>
<td>13.0859</td>
<td>6.0810</td>
</tr>
<tr>
<td>5:3 Compressor</td>
<td>32.81</td>
<td>475.95</td>
<td>15.6159</td>
<td>7.4323</td>
</tr>
<tr>
<td>6:3 Compressor</td>
<td>43.14</td>
<td>606.45</td>
<td>26.1622</td>
<td>15.8660</td>
</tr>
<tr>
<td>7:3 Compressor</td>
<td>44.80</td>
<td>689</td>
<td>30.8672</td>
<td>21.2675</td>
</tr>
<tr>
<td>15:4 Compressor</td>
<td>248.78</td>
<td>1205</td>
<td>299.7799</td>
<td>361.2347</td>
</tr>
<tr>
<td>31:5 Compressor</td>
<td>322.6</td>
<td>2015</td>
<td>650.039</td>
<td>1309.8285</td>
</tr>
</tbody>
</table>

Fig. 6 Modified 15:4 compressor
Table III. MAC Comparison

<table>
<thead>
<tr>
<th>MAC unit</th>
<th>Power in mW</th>
<th>Delay in nS</th>
<th>PDP in nJ</th>
<th>EDP (10^-18 J·sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>32x32 MAC (Using proposed FA)</td>
<td>28.49</td>
<td>7.25</td>
<td>0.2065</td>
<td>1.4975</td>
</tr>
<tr>
<td>32x32 MAC (Using SERF FA)</td>
<td>37.62</td>
<td>7.23</td>
<td>0.2720</td>
<td>1.9674</td>
</tr>
<tr>
<td>32x32 MAC (Using CMOS 28T FA)</td>
<td>43.88</td>
<td>39.81</td>
<td>1.7479</td>
<td>69.5835</td>
</tr>
</tbody>
</table>

II. CONCLUSION

In this thesis paper, energy-efficient 32 bit multiply and accumulator (MAC) unit architecture has been presented. The architecture is based on reduced complexity modified Wallace tree architecture for optimal performance. Various multiply and accumulate (MAC) units were designed, simulated and analyzed for their performance and functionality. Use of Modified compressors helped in high speed computation in partial products summation stage of the Multipliers. It reduces the vertical critical path delay, which in turn reduces the number of stages required for partial products summation. The proposed low power full adder is used as the basic building block in these compressors and MAC units. The 32x32 bit MAC unit designed using proposed full adder as the basic building block gave a power saving of 24.27% over 32 bit MAC designed using SERF full adder and 35.07% power savings over 32 bit MAC designed using conventional 28T full adder. The MAC unit designed in this work can be used in FIR filter realizations for High speed DSP applications, in ALU of high speed microprocessors and can be a very useful block in ASICs and DSPs designed for many hand held devices such as Digital Hearing aid devices etc.

REFERENCES